Using CNTFETs and Ternary Adders for High Performance in VLSI- A Review

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Abstract: - With its lower chip footprint, faster processing times, and fewer connections to other components, ternary logic is a promising alternative to conventional VLSI binary logic. This article covers a few designs that employ CNTFETs (carbon nanotube field impact transistors) to produce a ternary half-adder. Many studies are now being conducted to better understand CNTFETs, their potential applications in logic gates, and whether or not they provide an efficiency boost over more traditional MOS technology. Multi-appraised logics, as well as binary and ternary memory cells, are all part of the CNTFET circuit's implementation. Information route circuits, such as the adder circuit, may benefit greatly from the use of one of the suggested ternaries to binary decoder circuits since it simplifies the circuit's subsequent execution and results in considerable delay and energy savings. Extensive Modeling using HSPICE allowed for the improvement of product strength, latency, and energy-delay in these circuits.

Keywords: - carbon nanotube field impact transistors, MOS technology, adder, ternary half adder, delay, energy-delay

Introduction: -

The unique structures and extraordinary physical qualities of carbon nanotubes have attracted a lot of attention in the field of electronics during the last several decades thanks to CNT technology. The carbon nanotube field effect transistor (CNTFET) is a unique device made by replacing the conventional silicon channel region of a field effect transistor with CNTs[1]. CMOS transistors are reaching their limitations and will need to be replaced by new, emerging technologies if we want to keep downsizing our features. CMOS transistors have various drawbacks, such as a short channel effect, poor gate control, excessive leakage power, and variable parameters [2]. Due to its ability to scale in size, the complementary metal oxide semiconductor (CMOS) method has been the standard technology for VLSI circuits and systems for the last several decades [3, 4].

CNT field-effect transistors (CNTFETs) with CNTs of different diameters (and hence chirality) may be used to create a multi-threshold design. There have been a number of presentations of ternary logic circuits employing CNTFETs and resistive loads [3, 4, 5, 6, 7, 8, 9, 10, 11]. However, massive OFF-chip resistors (with values of at least 100 M) are necessary for this configuration because of the high current needs of the CNTFETs. In this study, we propose a technique for designing ternary logic gates that operates under active load and does away with the requirement for large resistors by making use of p-type CNTFETs. [4] Evaluation and comparison with other published multivalued logic architectures based on CNTFETs with different numbers of thresholds are performed. As an alternative to CMOS, the CNTFET has been developed. The complementary metal-oxide-semiconductor field-effect transistor (CNTFET) has several characteristics with the complementary metal-oxide-semiconductor field-effect transistor (CMOS), including device construction and operating mechanism [6].

Literature review: -

Design and analysis of ternary full adders and multipliers are offered as examples of the practical use of the concepts described in this article for designing basic ternary gates/operators (inverters, NAND, and NOR). In order to boost processing speed without significantly increasing power consumption, a modified ternary logic circuit design technique is used for the arithmetic circuit design. The modified ternary logic design uses both ternary logic gates and binary logic gates, the latter of which are derived from the ternary logic design structures used in the former. While binary logic gates are ideal for fast computation [1], ternary logic gates make a great option for the decoding block due to their reduced gate count.

Two novel circuits for ternary half adders are demonstrated that make use of the more advanced CNTFET devices that have recently been produced, and the paper is titled "A ternary adder using CNTFET." The most well-known half-adder circuit based on the CNTFET minimal model of Stand passing is compared in both HSPICE and the circuit displays. Tests have shown that the recommended reasoning circuits are superior to the alternative design in terms of reducing power consumption and minimising delays. One of the novel structures created by the authors (Design2) reduces latency by 9%, power consumption by 63%, and PDP by 66%. This adder may be configured in a fashion that allows for the use of state-of-the-art CNTFET devices, similar to those used in quantum computers, allowing for the creation of complex number-juggling circuits.

A better compressor than the one before it is claimed in a study titled "Superior Ternary (4:2) Compressor Based on Capacitive Threshold Logic" by Reza Faghih Mirzaee and others. The ternary (4:2) blower is discussed here, since it plays a crucial role in the design process. However, the ternary model is distinct from the parallel one in that it does not rely on the transmission of signals to function. The output flags may be easily retrieved using CTL. The capacitor organisation is also divided in half, although not as dramatically as the preceding arrangement. This isolation makes the system more stable and resistant to PVT (process, voltage, temperature) fluctuations. HSPICE was instrumental in the development of 32nm CNFETs. According to the findings of the replication, the new architecture improves the execution of power-postponed items (PDIs) by a factor of 94%.

It was M in this instance [3]. Alla Derakhshan, Ali Derakhshan, Ali Derakhshan, Ali Derakhshan, Ali Derakhshan, Ali Derakhshan, and Ali Derakhshan. Derakhshan, all of whom contributed to the project, A CNFET designed in the style of a ternary multiplier. This paper proposes a method to improve Carbon Nanotube Field Effect Transistor (CNTFET) technology by using unary administrators of multivalued logic. The famous Wallace multiplier might serve as a model for this project. It's a novel ternary multiplexer design that just requires a small number of CNTFETs to implement. Two ternary full-adder topologies are also shown, one after examining the multiplier's architecture and the other. Compared to a continuous design, the number of CNTFETs is cut by 67% thanks to the employment of a single trit multiplier and a second multiplier. HSPICE simulations demonstrate that the various drive excellence strategies all include a low-power deferment component. However, the structures are eerily similar to past works that explored the same chaotic edge.

The contributors to this research (numbering four) came up with the name "Excellent CNFET-based Ternary Full Adders," and that's what it's known as. The purpose of this study is to investigate the feasibility of constructing ternary complete adder cells using carbon nanotube field effect transistors (CNFETs). They've been designed to make use of the cutting-edge properties of CNFETs, such as adjusting the distance between CNFET gates to get the desired voltages. HSPICE test equipment, which uses 32 nm CNFET technology, is used to verify the functionality of the proposed circuits. The proposed methods have been tested and shown to be effective in a variety of settings, including those with wildly varying voltages, temperatures, and operating frequencies. Tests show that the proposed designs outperform the quickest ternary full adders based on CNFETs.

There is a research article titled "Structure and Development of a Low Power Ternary Full Adder" that discusses the design and implementation of such an efficient and low-power device. The adder's operation is also discussed. This work details the CMOS-based fabrication of a low-power ternary complete adder. Two major physical obstacles are the positive ternary inverter (PTI) and the negative ternary inverter (NTI). They are fabricated using a CMOS inverter and pass transistors, and their design is based on a ternary full adder. To improve their performance in PTI and NTI architectures, transistors' W/L ratios were modified. The MOSIS demonstration's ternary full adder and structural squares were given a realistic appearance with the help of SPICE 2G.6. The PTI's rise and fall times are 14 and 4 times faster, respectively, than those of prior structures built using exhaustion upgrade CMOS (DECMOS) technology. The NTIs reveal a multiplier between 4 and 17. Their commotion edges improve by a factor of two or three in PTI and NTI, respectively, compared to the baseline. The MOSIS CMOS technology was utilized to fabricate the ternary full adder. We compared the adder's overall behavior to that of the SPICE-like structure by inspecting its structural squares (NTI and PTI). How well it is functioning is of great importance to us. In contrast to the DECMOS breakthrough, the ternary-valued reasoning circuits in this research do not employ MOSFETS in consumption mode, making them more efficient. The new design [needed source] has microwatt-scale power dissipation, fewer components, and compatibility with state-of-the-art CMOS technology.

The title of the paper is "Low Power CNTFET-Based Ternary Full Adder Cell for Nanoelectronics" [6]. Seyyed Ashkan Ebrahimi, as well as other people, wrote this ""Low Power CNTFET-Based Ternary Full Adder Cell for Nanoelectronics," "Low

Power CNTFET-Based Ternary Full Adder Cell for Nanoelectronics," Ter Interconnecting Low Power CNTFETs makes up about 70% of the total area of a VLSI circuit. Due to the high density of occupied areas, there are many restrictions on how much and how often you can make and use parallel circuits. One of the best ways to make sure that important information and critical value can be passed on in paired frameworks is to use different, credible explanations. With the rise of small, flexible gadgets that need electricity, people are more likely to use low-power solutions. In this work, CNTFETs are used to make a new low-power ternary full adder cell that the authors argue for and evaluate in this paper (Carbon Nano-Tube Field Effect Transistors). The authors of this adder cell made it more effective by incorporating the good things about CNTFET into their design and execution. When compared to previous research, simulations with HSPICE show that the proposed TFA (ternary full adder) uses much less power and has a big impact on the amount of power that can be deferred.

VLSI chips need to be smaller and more efficient to function well in modern computerized time. There are fewer issues with the circuit and chip size if you use ternary reasoning rather than double reasoning. [7] Gaurav Agarwal, Gaurav, and all the other people who worked on this project Experiment with Ternary Basic Gates and Half Adders that are based on CNTFETs to see how well they work in real-world situations.

In a paper titled "Efficient CNTFET-based Ternary Full Adder Cells for Nano Gadgets," authored by Mohammad Hossein Moaiyer and his colleagues, they demonstrate two novel and efficient ternary Full Adder cells. These ternary Full Adders can be constructed with CNTFETs due to their unique characteristics, such as the ability to select the optimal edge voltages by accounting for a real distance across the nanotubes.

Structure of low-edge full adder cells with carbon nanotube field effect transistors; also seen as "Structure of low-edge full adder cells with CNTFET," "Structure of low-edge full adder cells with CNTFET," and so on.

[10] Manjunath Patil and other people wrote a paper called "Power Efficient Parallel Adder Design Using CNTFET Technology." This article shows how to make a Power Efficient Parallel Adder with a carbon nanotube field-effect transistor. When compared to the traditional parallel rationale structure strategy, the ternary rationale structure strategy is more flexible. This is because the current computerized plan lets you look at energy efficiency and ease of use because the circuit has less chip space and interconnections. It is supposed to be used to do ternary logic that is CNTFET-dependent. Instead of the resistive burden CNTFET logic gate structure, it will be used. The author can infer that the circuit, which has a multiplier and a complete adder, is very efficient and fast because it has a ternary logic gate system and a double gate process structure. Before, the CNTFET was done with a resistive load. The proposed ternary reasoning gates have a delay and low power consumption. They include Fin-Field Effect Transistors, Single-Energy Transistors, and Silicon on Insulator. These are some of the most recent changes to CNTFET.

[11] There are a lot of people named Balaji Ramakrishna S et al. Balaji Ramakrishna S et al. A new 14t adder cell with CNTFETs has been made for low-power computing. The goal of this study is to make a 14-transistor one-piece adder cell with CNTFET 32nm Technology in order to deal with power and speed issues that come with elite computing frameworks. An adder cell's performance is compared to that of other full adders, such as an ordinary full adder and one with a transmission gate and CNTFETs. The suggested method takes less time and doesn't use a lot of energy at all. The one-volt power source and single-walled carbon nanotubes are used to power the construction. It uses the Stanford library of 32nm planar CNTFETs and is shown with a one-volt power source. This is how it works: On the adder cells we're looking at, we've done a lot of reproduction. We're now looking into things like power, postponement, and PDP in more detail. To make sure that the 14T adder cell is strong, the effect of temperature on its power consumption is also looked at. Replication results show that the proposed adder can keep its output drivability at the same level while significantly reducing leakage power.

[12] Fazel Sharifi and other people's work is called "A New Quaternary Full Adder Cell Based on Nanotechnology." People who make circuits based on binary logic can't make them work because they need to connect things. Some people might use credible arguments to send more data over a flag line, which would be a good strategy (MVL). This research shows how to make a high-performance quaternary complete adder cell by using a carbon nanotube field effect transistor, which is a type of transistor (CNTFET). The suggested Quaternary complete adder can be built in a number of voltage ranges that people like. CNTFET is a possible replacement for the MOSFET. It has a lot of advantages, like the ability to change the width of the nanotubes to get the best edge voltage, which makes them good for multiple voltage mode edge circuit designs. In Synopsys HSPICE, it is looked at with standard 32 nm CNTFET technology and at different temperatures and voltages, with the recommended circuit as the test bed.

In this study, we offer an experimental design for a ternary complete adder that employs pseudo-N-type carbon nanotube FETs to perform the necessary arithmetic operations, rather than conventional FETs. The more an Adder circuit's processing power, the greater its output, since larger numbers may now be recorded with greater prominence. The article explains how to design and implement a ternary adder, which operates on the basis of ternary logic. The structure is helpful for pseudo n-Type carbon nanotube field effect transistors, but only when such transistors are really implemented. This article uses the power consumption, deferral, and power postponement features of a ternary complete adder as an example to demonstrate these concepts.

This research, authored by Seyyed Ashkan Ebrahimi and colleagues, is titled "Low-power CNTFET-based Ternary Full Adder Cell for Nanoelectronics." About 70% of the entire area of a VLSI circuit is taken up by interconnections. There are several challenges to constructing and using double circuits because of the high density of inhabited zones. Using a range of plausible explanations is one of the finest strategies to facilitate the transfer of critical value and information between two frameworks. Low-power methods are becoming more important as the number of tiny, energy-hungry gadgets proliferates. In this research, the authors propose and rigorously evaluate the usage of CNTFETs (Carbon Nano-Tube Field Effect Transistors) in the construction of a revolutionary low-power ternary complete adder cell. The scientists improved the efficiency of this adder cell thanks in large part to the CNTFET characteristics. This becomes evident when comparing the planned TFA (ternary full adder) with earlier efforts. In order to promote further development in the domain of the power defers item, the suggested TFA (ternary full adder) consumes less energy.

The paper's title, "A Reversible Ternary Adder for Quantum Computation," was written by Takahiko Satoh and co-authors. Since qutrits, the ternary counterpart of parallel qubits, have been proven to be capable of storing a large amount of data in a relatively little amount of space, they have been suggested for use in quantum correspondence, including quantum key transfer (QKD). The premise set of the simplest quantum frameworks, termed quadrants, consists of three states, each of which is characterized by a set of three vectors. The authors state that |0i, |1i, & |2i constitute the premise set for ternary arithmetic. This is also the standard definition of a qubit. To do complex arithmetic on qutrits, it is probable that special subroutines will be required to manipulate large numbers. While instructions exist for constructing squares, improvements may be achieved by constructing larger and more complex circuits. What this signifies is that the writer has constructed a bidirectional adder circuit. This adder is modeled after the VBE carry-swell adder developed by Vedral, Barenco, and Ekert. The author's circuit doesn't carry out any quantum operations when employed in a conventional ternary rationale setting. It has been in use for a considerable yet atypically short period of time.

CNTFET:

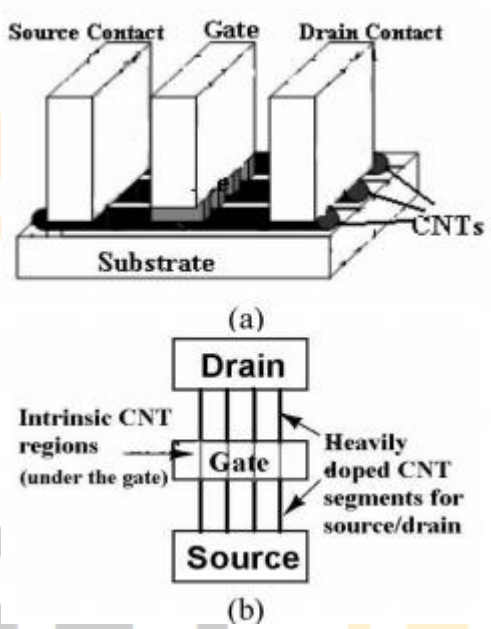

Figure 1: CNTFET (a) Schematic diagram (b) Top view

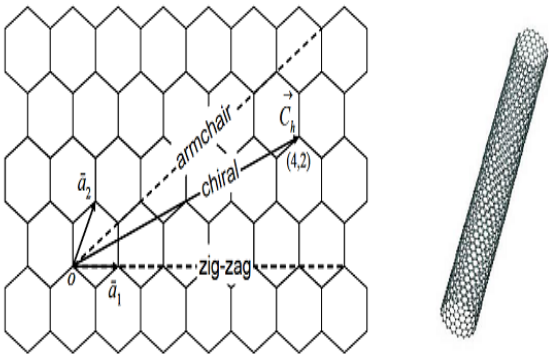

Figure 2: Unrolled graphite sheet and the rolled carbon nanotube lattice structure.

Carbon nanotube field-effect transistors (CNTFETs) are what you need to know about. In place of the bulk silicon used in a MOSFET, carbon nanotubes are used to create this field-effect transistor. There have been several developments in CNTFETs since it was originally shown in 1998. To create this one-dimensional structure, graphene sheets are rolled into cylinders. SWCNT is a useful material for fabricating CNTFETs [8], which are electrical devices. The chemical, mechanical, and electrical characteristics of CNT are exceptional. CNT's sp2

chemical bond provides it with exceptional strength. The carriers are directed in one way, minimizing the dispersion effect, and CNT requires less energy to operate. The chirality of SWCNTs determines whether they are metallic or semiconducting. The rolling angle of graphene sheets establishes N and M [7]. Some nanodevices that may one day replace bulk CMOS include the carbon nanotube field effect transistor, the single electron transistor, the graphene nanoribbon transistor, and the quantum-dot cellular automaton. When comparing all of these nanodevices, the CNTFET may stand out due to its similarities to the MOSFET in terms of its electrical operation. The CNFET is a viable alternative to CMOS transistors. Both CMOS and CNFET transistors are fairly comparable in terms of their electronic properties [4]. This suggests that CNFET might be a viable CMOS substitute without requiring extensive platform modifications. CNFET devices are suitable for rapid and low-power circuits because to their unique one-dimensional band structure, which eliminates backscattering and makes them nearly ballistic [8]. Scaling down Si FETs is challenging because of the short channel effect [9], which occurs when electrons are transported straight from the source to drain. The process of scaling up may be accomplished with the help of a CNTFET, a nanoelectronic device. Multiple thresholds are possible in MVL circuits [7]. Changing the voltage across the bulk terminal in CMOS allows for many thresholds, whereas in CNTFET, variable diameters are used for this purpose [2].

Ternary Adder: -

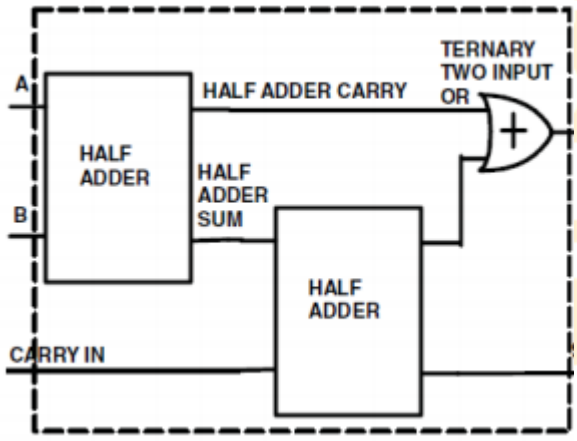

Figure 3: Ternary Full-Adder

A 1-bit ternary complete adder adds together two ternary values and a carry, denoted by Cin here, that has already been calculated. This circuit's output sum has a size of 2 bits and is represented by the signals Cout and SUM. Two ternary half adder circuits may be connected in series to form a ternary full adder. A ternary full adder block, as shown in Figure 4, is built from two ternary half adder blocks. In this case, the first half adder combines the two input bits A and B. Next, a half adder takes the sum of the A and B inputs and the preceding carry (Cin) as its input, and produces a sum bit and a carry bit. The final carry bit (Cout) is produced by the OR operation between the two carry bits produced in the two stages (first half adder and second half adder) [9]. Carbon nano tube field effect transistors (CNFETs) may be fabricated to resemble a flat sheet of graphite tubes. One of the benefits of CNFET transistors is that they have a higher ON current compared to MOSFET transistors. CNFETs provide a number of benefits in addition to their ability to achieve feature sizes smaller than are now achievable using lithographic methods. The decreased power dissipation in the transistor body due to ballistic conduction is an additional perk of CNFETs. Due to their one-dimensional structure, CNTs have a low resistance, resulting in minimal power dissipation and consumption [10]. Carbon nanotube field effect transistors (CNFETs) may be fabricated to resemble a flat sheet of graphite tubes. One of the benefits of CNFET transistors is that they have a higher ON current compared to MOSFET transistors. CNFETs provide a number of benefits in addition to their ability to achieve feature sizes smaller than are now achievable using lithographic methods. The decreased power dissipation in the transistor body due to ballistic conduction is an additional perk of CNFETs. CNTs' one-dimensional structure decreases their resistivity, which in turn reduces energy loss and power consumption [2]. Optimizing the performance of a 1-bit full adder cell contributes to improved electronic device performance since full adders are the essential building blocks of arithmetic operations in Very Large Scale Integrated (VLSI) circuits. Due to its unique mechanical and electrical properties (see Figure 1), carbon nanotube field effect transistors (CNTFET) have been shown to be the most acceptable replacement to metal oxide field effect transistors. (MOSFET). Carbon nanotubes (CNTs) are used to create the channel of the CNTFET transistor. Using CNTFET 32nm technology [3], a full adder cell is shown with high throughput, low power consumption, and a small number of transistors. The current drive of a CNFET device is identical to that of an N-FET device because of the CNFET's mobility being identical to that of a P-FET device. This makes it much easier to determine the optimal size for transistors in intricate circuits. Perhaps the most intriguing use of CNFET transistors is in Multiple Valued Logic (MVL). Using more than two logic values simultaneously is what is meant by "MVL logic" when constructing circuits and systems. CNFETs may be useful for designing MVL circuits. Since MVL is based on a multiple threshold design strategy, it is simple to determine how much more current can flow through

CNFETs by increasing the nanotubes' width. The large number of pins and interconnects needed, especially in small circuits, is a major challenge in binary logic. As a consequence of this problem, there is a limit on the total number of internal and external connections. The circuit may be made smaller by reducing the number of pins and the quantity of extra wiring between them. When compared to binary logic, MVL designs are quicker and need fewer computation steps because more information can be sent through the wires and interconnections. For MVL logic, a wide variety of radices are available. Most effectively, e (2.718) is used in the most fundamental operations of all radices. However, as real-number systems can't be implemented with today's technology, natural numbers should be utilised instead. Therefore, it is preferable to choose radix 3, which is the closest natural number to e. Ternary logic is superior because it reduces production costs and complexity [8]. Design and analysis of ternary full adders and multipliers are offered as examples of the practical use of the concepts described in this article for designing basic ternary gates/operators (inverters, NAND, and NOR). In order to boost processing speed without significantly increasing power consumption, a modified ternary logic circuit design technique is used for the arithmetic circuit design. The benefits of both ternary and binary logic gates are used in the modified ternary logic design [10], which is based on the original ternary logic design structures. To that end, designers are working to streamline logic circuits like adders, multipliers, and memories by cutting down on factors like latency, energy use, and connection complexity. As more and more modules are squeezed onto a single chip, on-chip interconnections have become increasingly challenging to establish. The bulk of a conventional binary circuit chip is taken up by the interconnects, with the insulation taking up 20% and the transistors just 10%. [9] These interconnects waste energy by raising the circuit's capacitance, resistance, and inductance, which in turn slows down responses and causes coupling effects.

Conclusion: -

Therefore, we provide this review article on High Performance Ternary Adder using CNTFET. Space, time, power, and noise are all factors that benefit from this technology's implementation. With the help of soon-to-be-available CNTFET hardware, two improved circuits for ternary half adders were developed. The performance of the circuit is compared using HSPICE simulations to that of the best known half-adder circuit, which is built on Sandford's CNTFET compact model. It has been proposed that two different high-performance ternary full adder cells based on CNFETs may be used. Using their individual strengths, the proposed circuits make full advantage of devices with multiple Vths. Reduced interconnections, faster processing times, and a smaller chip area are just some of the reasons why tenth-order binary logic has shown to be a viable alternative to traditional VLSI binary logic. Another viable alternative to traditional binary logic is tenth-order binary logic. By minimising the need for elaborate support circuitry like interconnects and chip regions, modern digital design may achieve simplicity and power efficiency. CNFETs.

Reference:

[1] Subhendu Kumar Sahoo et al., “High Performance Ternary Adder using CNTFET” DOI 10.1109/TNANO.2017.2649548, IEEE

[2] Reza Faghih Mirzaee, and Akram Reza et al., “High-Performance Ternary (4:2) Compressor Based on Capacitive Threshold Logic” INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2020, VOL. 63, NO. 4, PP.355-36

[3] A. Derakhshan, M. Imanieh, et al., “Design and Simulate ternary multiplier based CNFET” Scinzer Journal of Engineering, Vol 3, Issue 2, (2021): 22-28

[4] Fazel Sharifi, Atiyeh Panahi, et al., “High Performance CNFET-based Ternary Full Adders” Proc IEEE, vol. 91, no. 2, pp. 305-327, 2017

[5] A. Srivastava et al., “Design and Implementation of a Low Power Ternary Full Adder” November 29, 1993, Revised April 26, 2016

[6] Seyyed Ashkan Ebrahimi et al., “Low Power CNTFET- Based Ternary Full Adder Cell for Nanoelectronics” 2231-2307, Volume-2, Issue-2, May 2012

[7] Gaurav Agarwal, Amit Kumar, et al., “Performance Evaluation of CNTFET Based Ternary Basic Gates and Half Adder” Volume 5 Issue 5, May 2016

[8] Mohammad Hossein Moaiyer et al., “Efficient CNTFET-based Ternary Full Adder Cells for Nano electronics” Received 27 Feb 2011; accepted 11 April 2011; published online 19 April 2011

[9] P Chandrashekar et al., “Design of low threshold Full Adder cell using CNTFET” Research ISSN 0973-4562 Volume 12, Number 12 (2017) pp. 3411-3415

[10] Manjunath Patil et al., “Power Efficient Parallel Adder Design Using CNTFET Technology” ISSN: 2348-4748, IJEEE Volume 2, Issue 4, April 2015

[11] Balaji Ramakrishna S et al., “CNTFET Based Novel 14t Adder Cell for Low Power Computation” ICTACT Journal on Microelectronics, October 2017, VOLUME: 03, ISSUE: 03

[12] Fazel Sharifi et al., “A Novel Quaternary Full Adder Cell Based on Nanotechnology” I.J. Modern Education and Computer Science, 2015, 3, 19-25

[13] Kazi Muhammad Jameel et al., “Experimental Design of a Ternary Full Adder using Pseudo N-type Carbon Nano tube FETs” International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056 Volume: 02 Issue: 09 | Dec-2015

[14] Seyyed Ashkan Ebrahimi, et al., “Low Power CNTFET-based Ternary Full Adder Cell for Nanoelectronics” International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-2, May 2012

[15] Takahiko Satoh et al., "A Reversible Ternary Adder for Quantum Computation" Arxiv preprint quant-ph/0511084; to appear. Review Letters, 92(9):097901, 2004