# Enhanced Energy-Efficient D Flip-Flop using Graphene Nano Ribbon Field Effect Transistor (GNRFET) in 22nm Technology with Sleep Mode

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**Abstract-** The D flip-flop is very important in the applications of storage and circuitry, and its development leads to the enhancement of power-delay products (PDP) as well as power characteristics. The current body of research has suggested a variety of static and dynamic D flip-flops, but the most effective use of energy and power has not yet been accomplished. This thesis offers an effort to change the existing D Flip-Flop utilizing Graphene Nano Ribbon Field Effect Transistor (GNRFET) in the 22nm technology channel. The goal of this modification is to conserve energy by introducing a Sleep Mode idea, which prevents energy from being wasted via wasteful dissipation. According to the results of the circuit's simulations run in the HSPIce program, the suggested circuit has shown that it has higher performance in terms of mean power, time delay, and energy dissipation. The voltage source dissipation provided by GNRFET designs is almost indistinguishable from, and noticeably superior to, that provided by bulk CMOS MOSFET equivalents. As a result, GNRFET demonstrates itself to be an effective alternative to channel length technologies that fall within the 22nm group.

**Keywords:** *D Flip-Flop, Graphene Nano Ribbon Field Effect Transistor (GNRFET), 22nm technology, Sleep Mode, energy efficiency, power-delay product (PDP)*

## Introduction

The D flip-flop is an important memory cell that is used in digital circuits and is an important component overall. This is because it is capable of switching between two different states at will. It is also often employed in digital integrated circuits and in huge flip-flop arrays since it has such a wide variety of uses. This is because it has such a broad range of applications. The relevance of developing new D flip-flops and improving existing ones has been steadily rising over the last several years as a response to the ongoing pace of technological innovation as well as the increasing complexity of digital circuits. This is a reaction to both of these factors. This is due to the fact that both of these causes are contributing to the complexity that is being seen in digital circuits. This study proposes to improve the performance of D flip-flops by using Graphene Nano Ribbon Field Effect Transistors (GNRFET) in the 22nm technology channel and by creating a Sleep Mode idea in order to lower the amount of energy that is lost when the device is running. The purpose of this research is to reduce the amount of energy that is lost when the device is functioning. These two approaches are being considered in an effort to cut down on the quantity of electricity that is being squandered.

Despite the fact that the current body of study has suggested a number of unique static and dynamic D flip-flops, the most effective utilization of energy and power has not yet been accomplished. Within the boundaries of this thesis, we make an effort to find a solution to this problem by bringing more refinements to the power-delay product, taking use of the distinctive operating modes made accessible by GNRFETs, and lowering the total number of transistors. In doing so, we hope to discover a way to find a solution to this issue. The idea that high-performance TSPC D flip-flops may be constructed by making use of GNRFET technology was the impetus behind this specific area of research. If we are successful, the devices that are produced will have a power-delay that is much reduced, and their energy efficiency will be significantly enhanced, making them a fantastic option for high-speed digital integrated circuits.

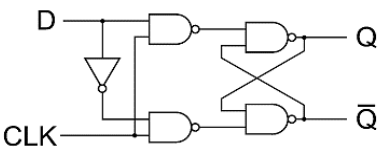


**Figure 1: DFF**

The primary objectives of this study are to develop an accurate and efficient system using GNRFET in dynamic DFF, to design a low power circuit with Sleep Mode to prevent short circuit power consumption, to create a high-speed D flip-flop using GNRFET in 22nm technology for a variety of applications, and to design an energy-efficient TSPC D flip-flop using GNRFET. All of these objectives will be accomplished through the use of GNRFET. Other objectives include the creation of a low-power circuit with a sleep mode, which will limit the waste of power through short circuits. The effective achievement of these goals will be made possible with the creation and application of a high-speed D flip-flop.

The primary purpose of this investigation will be to design and construct an improved D flip-flop that makes use of GNRFET in the 22nm technology channel. This will be the study's end goal. This will serve as the primary focus of the investigation. In order to illustrate the benefits of the design that has been proposed, it will be compared to alternative ways in terms of the amount of energy it consumes, the amount of time it takes, and the amount of energy it wastes. The results of this study will lead to the creation of D flip-flops that not only have a high degree of performance but are also efficient in terms of how they utilise the energy that they use. The use of these flip-flops is going to be necessary for the operation of digital circuits. This will make it possible to design more complicated devices that are also mindful of the amount of power they use. This is especially significant in the area of portable electronics, where it is very critical to have a low level of power consumption. This will make it possible to create more complex devices that are also conscious of the amount of power they consume.

In a nutshell, the purpose of this study was to enhance the performance of D flip-flops that make use of GNRFET in the 22nm technology channel while simultaneously enhancing their energy efficiency. This will be accomplished by putting into practice a strategy known as Sleep Mode, which has the goals of conserving energy and reducing the amount of dissipation that is unnecessary or excessive. The findings of this research will have a substantial influence on the growth of the portable electronics sector, the dissemination of information on devices that have a low impact on the environment, and the creation of new digital circuits for more complex computing.

**Previous work**

[1] Jahangir Shaikh and his colleagues conducted research to determine whether or not it would be possible to build PET scanners utilizing low-power D flip-flops. Imaging is critical for many different uses in medicine, including diagnosis and therapy. They created a seven-bit preset-competent dark code counter by using UMC 180nm CMOS technology, and they proposed a design for an MTSPC D flip-flop that requires an additional PMOS in order to prevent excessive flipping in the center regions. Both of these accomplishments were accomplished by employing the technology.

[2] Naresh Kumar and his coworkers came up with a novel architecture for a low-voltage D flip-flop, which blends DTMOS with a Bistable Gated Bipolar Device (BGB). This makes it possible to operate at a very low voltage while also shortening the response time. The leakage current that sleep transistors create is reduced thanks to this design, which in turn results in a reduction in the amount of power that is used.

[3] Himanshu Kumar and his coworkers investigated and analyzed a wide variety of D flip-flop circuits, giving special attention to the designs of push-pull partition D flip-flops. They simulated the circuits by using a 32nm SPICE process library, and they took into account the consequences that variations in process, voltage, and temperature had on delay performance.

[4] During the course of their conversation, M. Arunlakshman and his colleagues emphasized how important it is to take power dissipation into consideration while designing VLSI circuits and control systems. They investigated the challenges involved in reducing power consumption while maintaining performance levels, placing a focus on the need for VLSI circuits to achieve a balance between power expenditure, speed, and space usage in their research.

[5] Huei Chaeng Chin and his colleagues investigated the performance of GNRFETs and NMOSFETs in ULSI applications. They paid special attention to the energy delay product (EDP) and the power delay product (PDP) of each device. They made the discovery that GNRFETs have advantages over Si MOSFETs for short channel effects and give improved performance in digital logic circuits when the 16nm manufacturing technology is used. After doing comparisons between the two kinds of transistors, we came to this conclusion.

[6] N.D. Akhavan and his colleagues used three-dimensional quantum mechanical simulations to investigate the performance of doped GNRFET devices. In these simulations, the interactions that take place between electrons and phonons were taken into account. They arrived at the conclusion that doping not only makes GNRFET devices more compact but also enhances the performance of these devices.

[7] Yijian Ouyang and his colleagues explored the scaling behavior of graphene nano-ribbon (GNR) Schottky barrier field-effect transistors (SBFETs). They focused specifically on determining how well these transistors performed in contrast to Si MOSFETs. They found that GNR SBFETs had faster switching speeds; nevertheless, when scaled below 10 nm, these devices suffered from increased off-state leakage current. This was a problem for the devices.

[8] Abhijith A. Bharadwaj and his colleagues analyzed the performance of 6T SRAM cells constructed using FinFET, CNFET, and GNRFET technologies and discovered substantial disparities between the three methods. They evaluated the performance of a variety of SRAM architectures by taking into consideration the read delay, the write delay, and the power delay factors. To do this, they used HSpice and CosmoScope simulations. Read and write delays are both variables in the power delay.

[9] Kumari and Praveena investigated the design of 16-bit ripple carry adders and carry skip adders, as well as their analysis of these adders, using the use of GNRFET technology. They highlighted the advantages of GNRFETs in terms of speedier operation and decreased power consumption, underlining how this makes them a possible alternative to conventional MOSFET designs. In addition, they emphasized the benefits of GNRFETs in terms of reduced power consumption.

## Implementation

GNRFET technology was used throughout the construction of the circuits for this research; the parameters for this technology are detailed in Table 1. These parameters are used in the process of coding the circuits in Synopsys HSPICE; however, this software does not include a schematic creator. Before the circuits are entered into HSPICE for encoding, they are first drafted on paper as node diagrams.

**Table 1: GNRFET Technical Parameters**

| Parameter | Description | Value |
|---|---|---|
| nRib | The number of GNRs in the device. | 3 |
| n | The number of dimer lines in the GNR lattice | 6 |
| L | Physical channel length. | 22n |
| Tox | Oxide Thickness between channel and substrate/bottom gate | 0.95n |
| sp | The spacing between the edges of two adjacent GNRs within the same device | 1n |
| dop | Source and Drain reservoirs doping fraction | 0.001 |

The circuits for the research study, including the TSPC-based D flip-flop and the modified TSPC-based D flip-flop, are implemented using GNRFET technology, as shown in Figures 2 and 3.

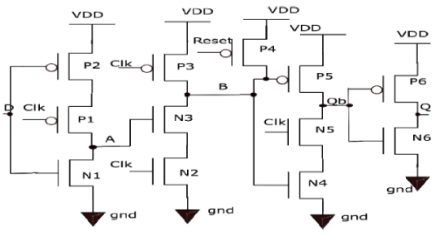


**Figure 2: DFF**

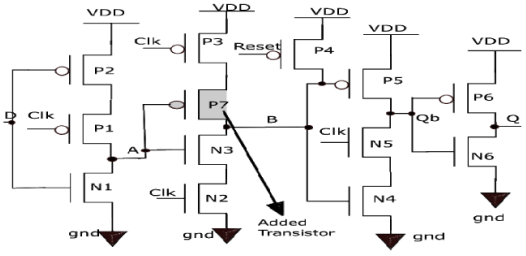

**Figure 3: MTSPC based DFF**

Figures 4 and 5 show the TSPC-based D flip-flop and modified TSPC-based D flip-flop implemented using GNRFET 22nm technology in LTSPICE. Figure 6 shows the proposed sleep mode for the modified TSPC-based D flip-flop circuit.

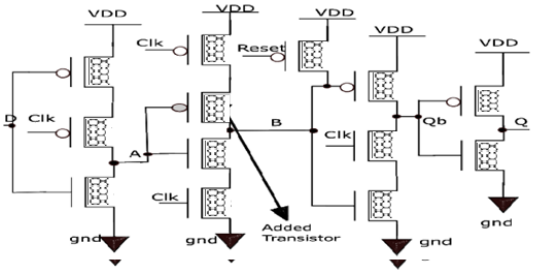


**Figure 4: TSPC DFF GNRFET**

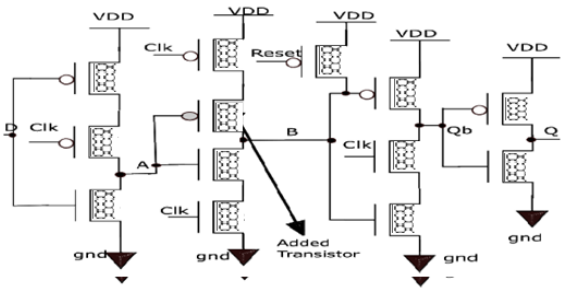


**Figure 5: MTSPC DFF GNRFET**

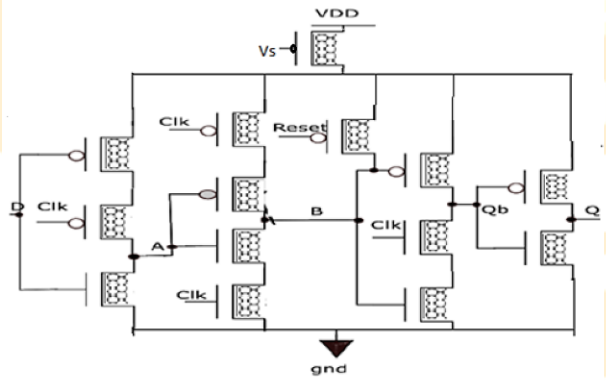


**Figure 6: MTSPC Sleep Mode DFF GNRFET 22nm**

**Results**

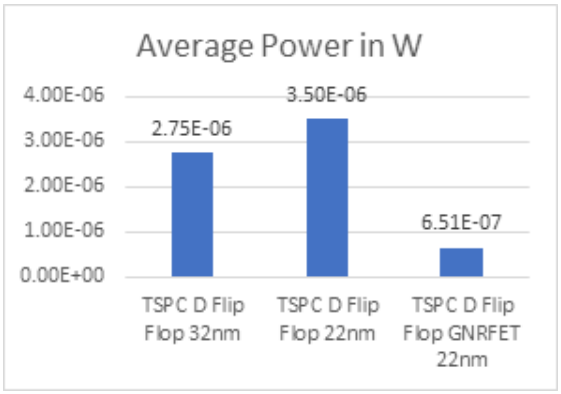


**Figure 7: Average Power for 32nm and 22nm TSPC DFF MOS and GNR**

Figure 7 shows that the TSPC DFF GNR based average power is lowest and 22nm MOS highest, which are the short channel consequences.

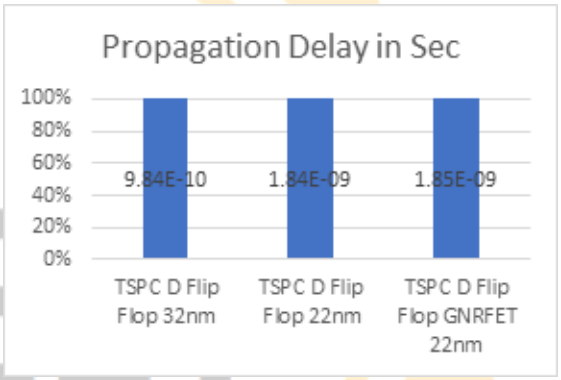


**Figure 8: Delay for 32nm and 22nm TSPC DFF MOS and GNR**

The delay case of GNRFET 22nm is considered to be the lowest on a single TSPC circuit in figure 8.

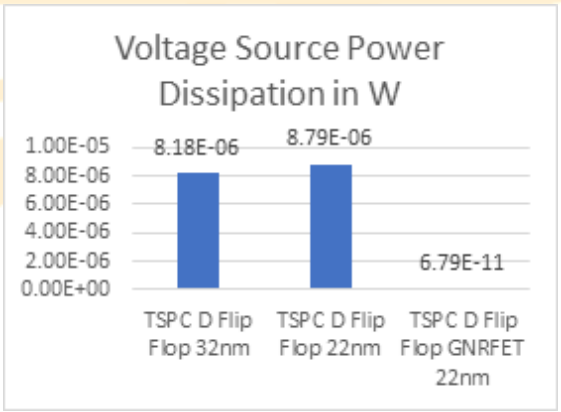


**Figure 9: Voltage Source Power Dissipation for 32nm and 22nm TSPC DFF MOS and GNR**

In Figure 9, the dynamic TSPC circuit based on GNRFET shows the lowest voltage power dissipation.

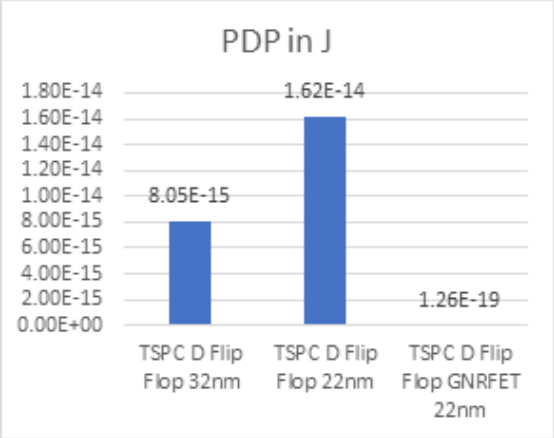


**Figure 10: PDP for 32nm and 22nm TSPC DFF MOS and GNR**

Figure 10 shows the PDP in DFF TSPC GNR as lowest and in MOS TSPC 22nm as highest.

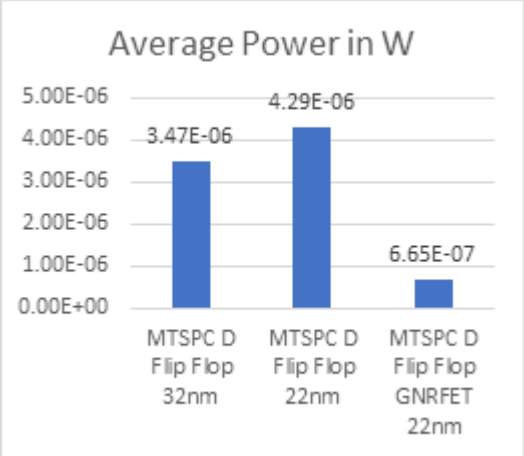


**Figure 11: Average Power for 32nm and 22nm Modified TSPC DFF MOS and GNR**

In the case of the upgraded TSPC D flip flop 22nm setup the average power and delay is also low in figures 11 and 12.

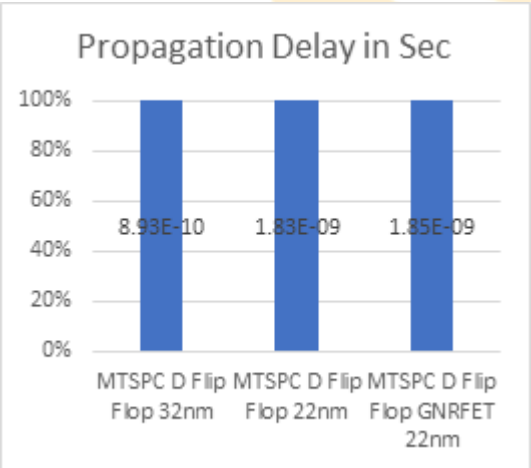


**Figure 12: Delay for 32nm and 22nm Modified TSPC DFF MOS and GNR**

In figures 13 and 14, 22nm modified are the lowest power and energy dissipation. DFF of TSPC.

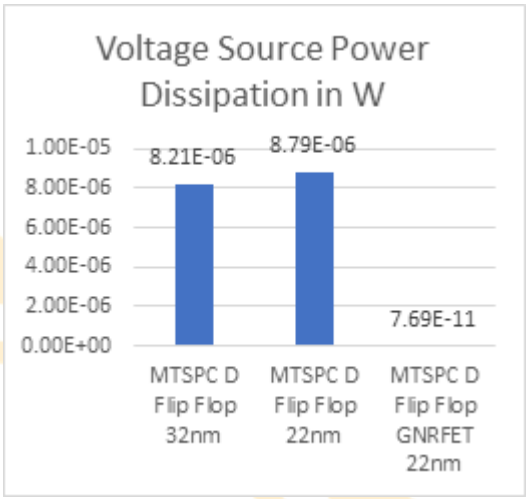


**Figure 13: Voltage Source Power Dissipation for 32nm and 22nm Modified TSPC DFF MOS and GNR**

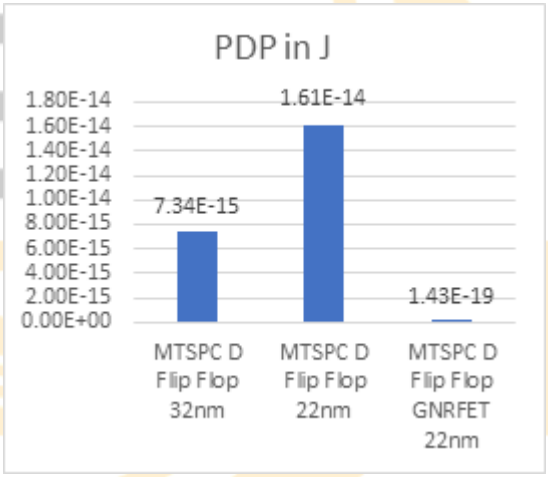


**Figure 14: PDP for 32nm and 22nm Modified TSPC DFF MOS and GNR**

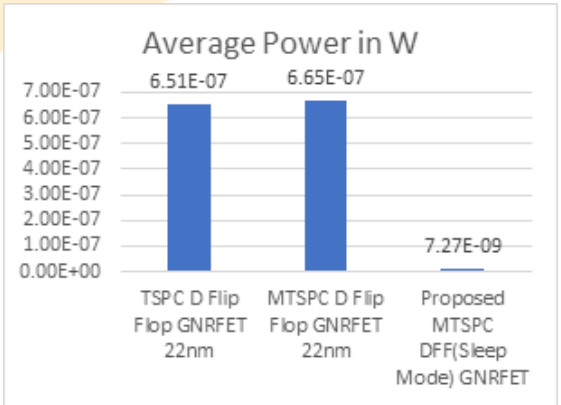

**Figure 15: Average Power for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR**

In the proposed TSPC D Flip Flop, the average capacity is better than in figure 16.

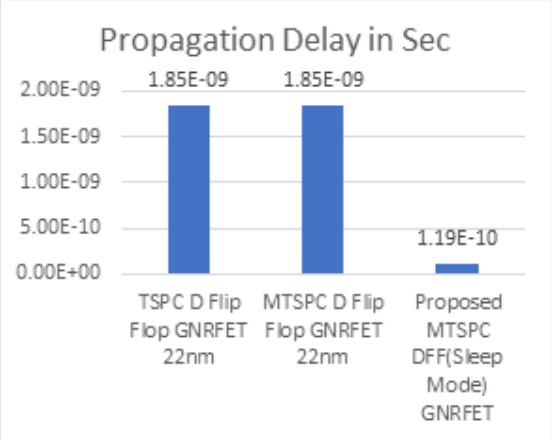


**Figure 16: Delay for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR**

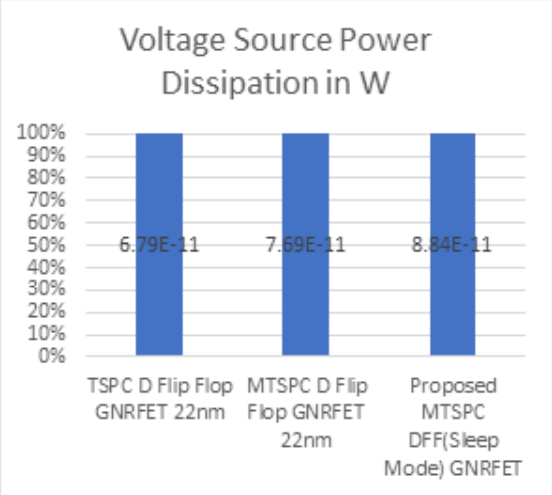


**Figure 17: VSPD for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR**

The power supply for all GNRFET-based circuits is almost the same, as shown in Figure 17, and this does not have a negative effect on the proposed circuit.

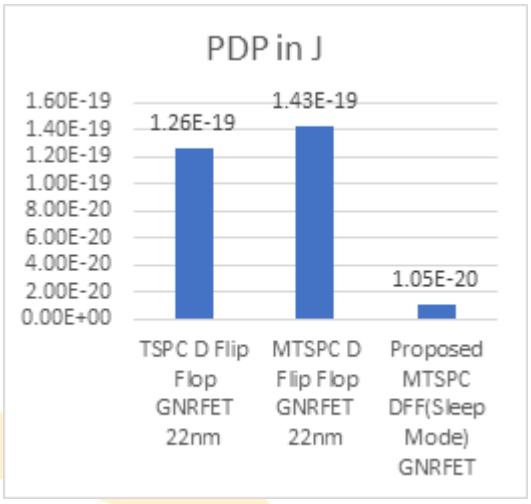


**Figure 18: PDP for 32nm and 22nm Proposed Sleep Mode based Modified TSPC DFF GNR**

In figure 18, the proposed circuit has the lowest PDP of 22nm of technical contributions in all GNR based circuits compared to the proposed.

## Conclusion

The results of the simulation show that making use of Sleep Mode reduces the typical amount of power consumed, increases the amount of time it takes for energy to be dissipated, and prolong the length of time it takes for the delay to accumulate. The voltage source power dissipation is almost same for each and every one of the GNRFET-based circuits. The findings of the experiment have been validated by both HSPICE and Avanwaves respectively. The time has been reduced by 97.9%, the power dissipation has been reduced by 99.9%, and the voltage source PDP has been adjusted by approximately 90%. The average power has grown by 96.55%. In combination with the GNRFET Sleep Mode technology, the Dynamic D Flip Flop adjustable circuit, which offers advantages such as low power consumption and high-speed optimization, may be put into use.

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