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DG-FinFET based ternary half adder for low-power applications

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Abstract- In this research, we examine a low-power ternary half adder that is based on DGFETs. This adder uses the devices. In this article, a ternary half adder that is low-power, low-leakage, and low-frequency is demonstrated with the assistance of a DGFET. There is one more interpretation that can be given for DGFET. The results of this study show that ternary adders with and without Double Gate Field Effect Transistors (DGFETs) have the same levels of latency, peak power distribution, and leakage power. This was discovered by comparing the two types of adders. When compared to deep submicron transistors, the technology known as Double Gate Field Effect Transistor, or DGFET, offers a number of distinct advantages. One of these benefits is the capacity to deal with short-channel events such as drain-induced barrier lowering, which can result in the failure of a transistor. This is just one of the many advantages that come along with using this technology. Because to the advancement of this technology, all electrical appliances now have increased intelligence and dependability as a result. It is probable that the results of this experiment will show a rise in the average power as well as the energy and power that has been dissipated.

Keywords- DG-FinFET, CNTFET, Ternary Adder, HSPICE

Introduction

Ongoing research and investigation are being conducted to learn more about the possible benefits of employing nonplanar transistor topologies, such as multigate designs and CNTFETs, for example. Using a single carbon nanotube that is put in an otherwise typical bulk MOSFET structure has the potential to lower these breakdown thresholds, and future reductions in device measurements are being promoted. This is because the application of bulk MOSFETs is developing into a more widespread practise. Professionals who specialise in the design of electronic devices and circuits, in addition to innovation, are presently concentrating their attention on the foreseeable future of the semiconductor industry in an effort to enhance the operation of the electronic framework. This is being done in the hope that it will result in an improvement in the functioning of the electronic framework. High-portability transistor channel materials are the subject of a substantial amount of research and development at the moment in order to provide more bearer flexibility. III-Visemiconductors are a type of material that fits under this category. Research is currently being carried out on a variety of new one-dimensional structures, such as carbon nanotubes (CNTs) and other structures of a similar nature. The high transporter mobility of carbon nanotubes (CNTs) has led to their emergence as a potential candidate to support the Siiinnovation agenda in the post-2015 time period. However, a number of obstacles still need to be overcome before this can come to fruition. The findings of the study indicate that next-generation field-effect transistors, which are also referred to as CNTFETs, make it possible to undertake research at both the device level and the circuit level. When the channel length of a MOSFET has been lowered to fewer than 10 nanometers, it will be impossible to make any further development in silicon-based technology by the year 2020. This is because silicon-based technology will have reached its theoretical limit. Because of this, the industry that deals in semiconductors is constantly on the lookout for cutting-edge discoveries in other materials and technologies that may complement or even replace the innovation that is currently based on silicon. Carbon nanotubes, often known as CNTs, are a relatively new material that has lately come to light as having the potential to be beneficial among the many other patterns that have been researched. Single-electron burrowing (SET), quantum cell automata (QCA), rapid single-transition quantum reasoning, and carbon nanotubes (CNT) are some of the architectures that fall under this category. They have an average diameter that falls somewhere between 1 and 3 nanometers, but their length can be several microns or possibly be far longer than that. Carbon nanotubes, also known as CNTs, are an intriguing material that could be put to use in the manufacture of a wide range of practical tools. Low-cost, high-quality connections, adaptable Carbon nanotube field-effect transistors (CNTFETs), and single electron penetrating transistors are a few examples of the types of devices that fall under this category. Several research groups from all over the

world are finally investigating CNTFET devices and the practical uses that they have. These investigations are taking place in mechanical labs and universities (IBM, Intel, and Infineon), as well as educational organisations (schools). These kinds of organisations are conceivably located in any part of the world (Purdue, Stanford, etc.). One of the most innovative ideas is to use complementary metal oxide semiconductor field effect transistors (CNTFETs) rather than silicon metal oxide semiconductor field effect transistors (MOSFETs). This is because CNTFETs are better able to handle the complementary metal oxide semiconductor field effect. In spite of the fact that it may be challenging to get accessible device models that are also suitable for particular structure streams, it is essential to own such models in order to create circuits that are dependent on particular devices. In this paper, a comprehensive analysis of a wide variety of currently available CNTFETs and numerous models that have undergone optimisation is presented. In order to examine the influence of the elements on the characteristics of the device, we made use of models that were available to the public and were easy to recreate. This enabled us to acquire results that were more accurate. Therefore, the current dimension and edge voltage of the CNTFET are both affected by the cylinder width, but the current dimension of the CNTFET is simply affected by the contact resistance. This is due to the fact that the current size of the CNTFET is controlled by the width of the cylinder. In order to build reliable circuits and networks, a circuit planner needs to be able to take into account a variety of elements at a variety of points across the circuit or network. In this particular illustration, the lengths of the nanotubes are the criteria that are being taken into consideration.

It wasn't until 1989 that a "fully double gate FET" was created, which the makers of the device at the time referred to as a "doubled gate SOI framework." This structure was comprised of not just one but two distinct sets of gates. This was the very first instance of a structure that was equivalent to a Double Gate Field Effect Transistor (DGFET) being displayed in its earliest form. This was also the very first time that this event took place. The year 1960 was the one in which this incident took place. Over the course of the past decade, it has been shown that the short-channel conductivity of planar MOSFETs has decreased. This trend was first observed in 2005. Consequently, there has been a rise in interest in Double Gate field Effect Transistors (DGFETs) within the same time period as a result of this trend. Double Gate Field Effect Transistors (DGFETs) offer a greater short-channel performance compared to planar Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) that have the same channel length, as shown in Figure 1. The amount of channel length in each of these two varieties of transistors is same. Figure 1 depicts a Double Gate Field Effect Transistor, or DGFET for short, in its normal planar configuration. This type of transistor is also known as a DGFET.

Double Gate Field Effect Transistor (DGFET) depicted in Figure 1.

The channel of the planar Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is horizontal, but the channel of the vertical Double Gate Field Effect Transistor (DGFET; sometimes known as a fin) is vertical. Because of this, the width of the Double Gate Field Effect Transistor (DGFET), which is denoted by the symbol "W," will be directly influenced by the height of the channel, which is denoted by the symbol "HFIN."

Implementation

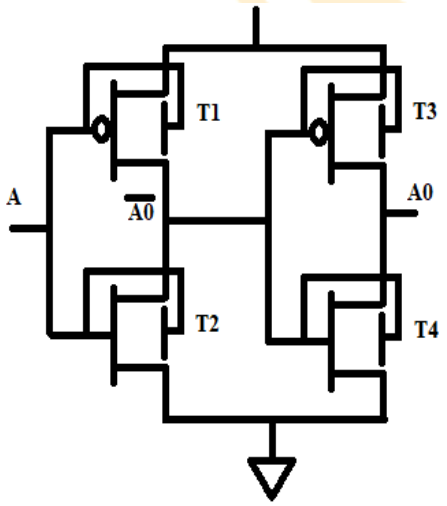

Fig. 2: Ternary Decoder using Double Gate Field Effect Transistor (DGFET)

Double Gate Field Effect Transistors, or DGFETs for short, are the components that make up the decoder circuit that was shown in the preceding image. This circuit can also be referred to by its other acronym, DGFET. The letter A represents the input to the decoder circuit, and the letter A0 represents the output of the circuit. Both letters are displayed in the diagram. The A0 and A0 bars are both produced

by this circuit in their respective forms.

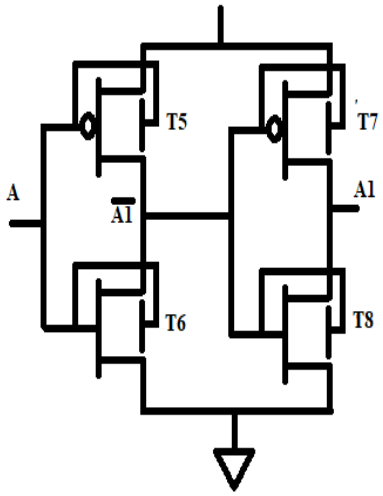

Fig. 3: Ternary Decoder

The decoder circuit that is depicted in Figure 3 is the same one that was depicted in Figure 2, with the difference that in this particular instance, we are using this circuit to create A1 and A1bar signals rather than simply A1 signal alone.

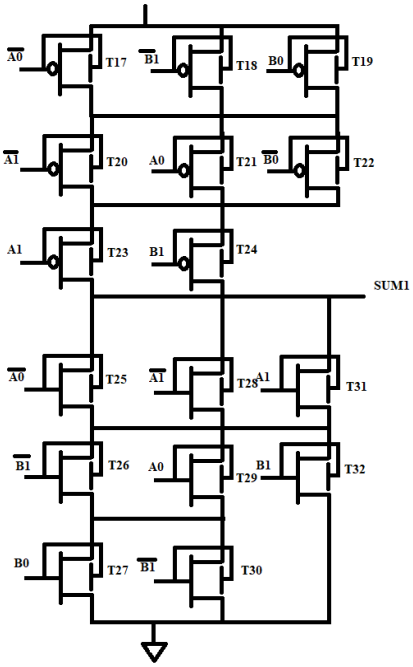

Fig. 4: Sum part 1 circuit

In this specific case, we will be constructing it with the help of sum1, and the result that the circuit will produce will be binary. The graphic that can be seen above has the circuit for a sum generator, which can be viewed there.

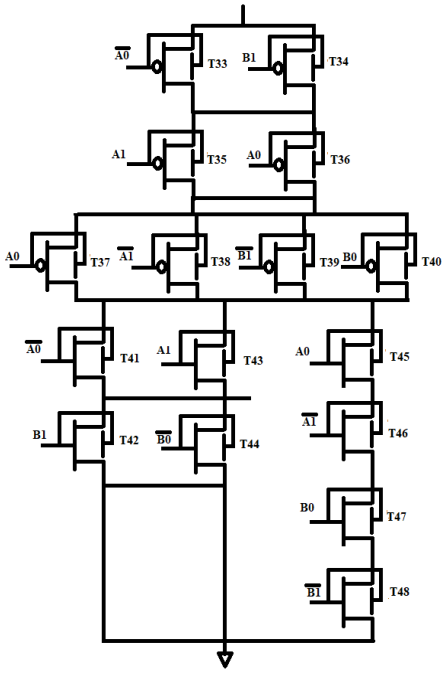

Fig. 5: Sum part 2 circuit

Figure 5 shows a representation of the sum generator; at the moment, we are working on sum2, and the output that we are obtaining is binary. In the current situation, we are working on sum2.

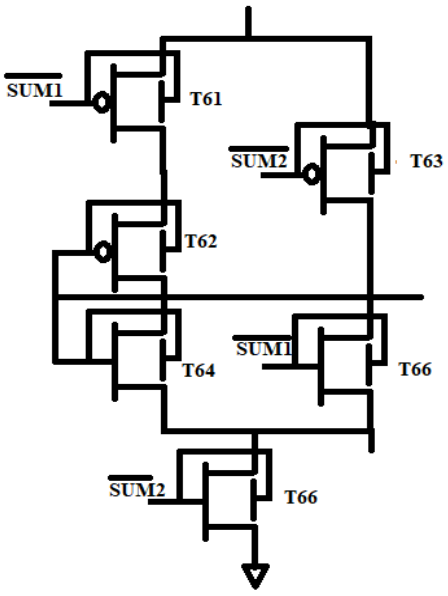

Fig. 6: Sum final circuit

Figure 6 depicts the circuit for a sum generator encoder; the output of the encoder is the addition of sum1 and sum2; this adds up to the final ternary output. The circuit for a sum generator encoder can be viewed here.

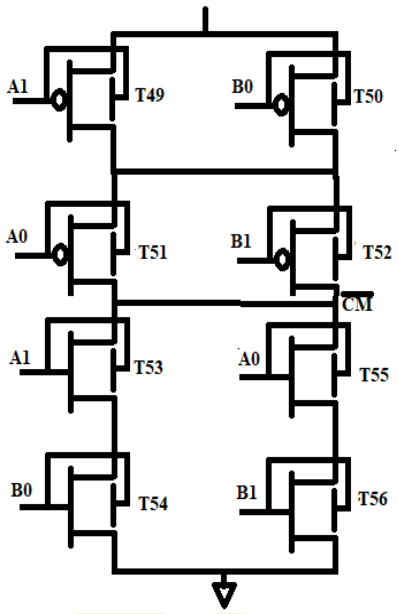

Fig. 7: Carry part circuit

Figure 7 depicts the circuit for the carry generator Cm, which makes use of both the p channel Double Gate Field Effect Transistor (DGFET) as well as the n channel Double Gate Field Effect Transistor (DGFET).

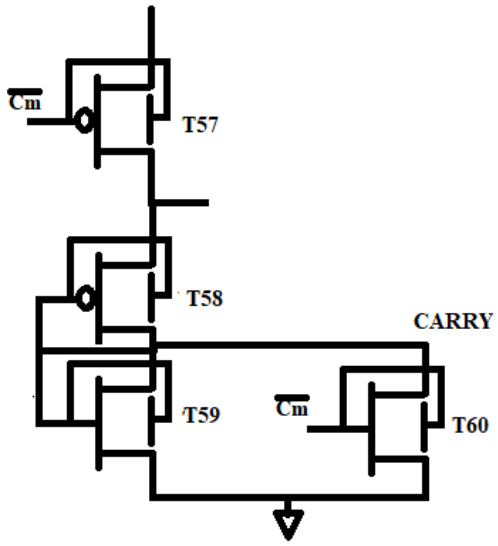

Fig. 8: Carry circuit

The carry is calculated with the help of the carry encoder circuit, which is illustrated in the picture that comes after this one. The circuit that creates the carry is depicted in the figure that comes before this one.

Results

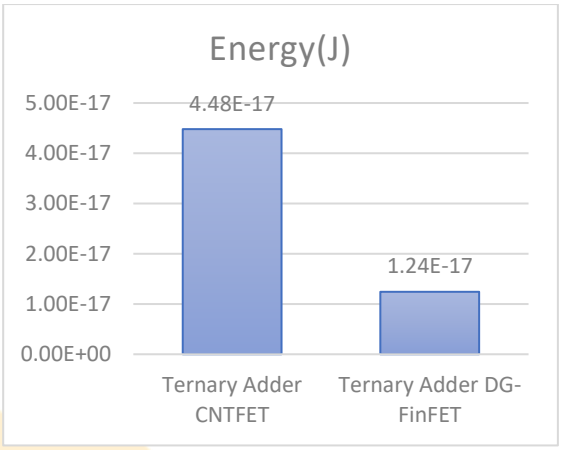

Fig. 9: Energy Result

Figure 9 is a representation of the amount of energy that would be generated by the suggested technological solution. When compared to the energy contained within the ternary adder Double Gate Field Effect Transistor (DGFET), the energy contained within the ternary adder CNTFET is much more than the energy contained within the ternary adder DGFET (DGFET).

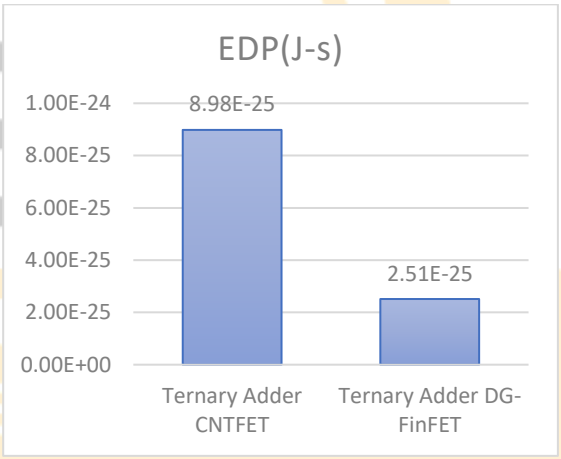

Fig. 10: EDP result

The EDP of the system that has been presented can be found shown in Figure 10. This figure depicts the EDP in the ternary adder CNTFET as having a very substantial size, as can be seen in the accompanying diagram.

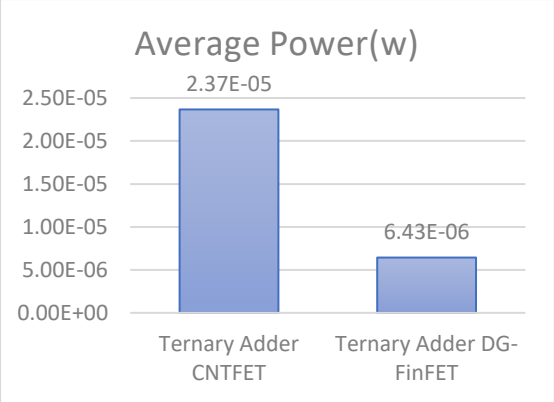

Fig. 11: Average Power results

In the ternary adder CNTFET, the average power of the suggested system as well as the average power are both bigger than they are in the ternary adder Double Gate Field Effect Transistor (DGFET), respectively. This is true not just for the average power but also for the average power.

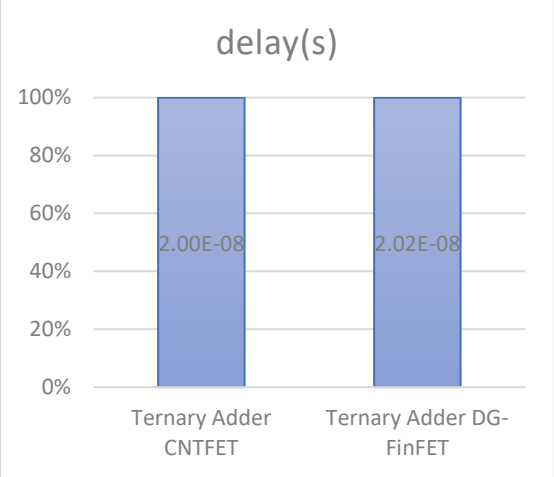

Fig. 12: Delay result

The above picture provides an illustration of how far behind schedule the planned system would operate for. The table that follows offers an example of the multiple comparisons that can be made between the ternary adder CNTFET transistor and the ternary adder Double Gate Field Effect Transistor (DGFET) transistor. These comparisons may be found in the following paragraphs. The result of the electricity being dissipated may be seen in figure 13.

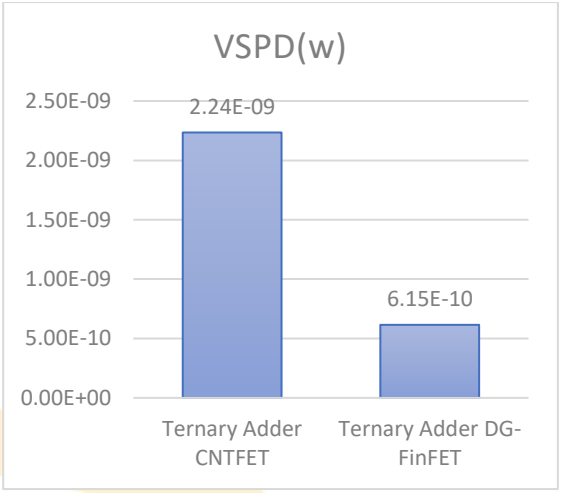

Fig. 13: Power dissipation result

Table 1: Output

	Ternary Adder CNTFET	**Ternary Adder DG-FinFET**
Average Power(w)	2.37E-05	6.43E-06
delay(s)	2.00E-08	2.02E-08
VSPD(w)	2.24E-09	6.15E-10
Energy(J)	4.48E-17	1.24E-17
EDP(J-s)	8.98E-25	2.51E-25

Conclusion

As a direct consequence of this, we have developed a low-power ternary half-adder by using a technique that is known as a double gate field effect transistor (DGFET). This was accomplished by combining two existing technologies. We have used a wide range of technologies, the most notable of which is a component that is referred to as a Double Gate Field Effect Transistor (DGFET). A method known as Double Gate Field Effect Transistor, or DGFET for short, is required in order to increase the power, latency, peak-to-average power, and leakage power of a ternary half-average adder. This may be accomplished by the usage of a DGFET. As can be seen from the information that was provided, we are contrasting the ternary adder Double Gate Field Effect Transistor (DGFET) with the ternary adder CNTFET, and we are doing so by using two separate circuits. This is something that can be observed by comparing the data that was provided. This is observable given the data that was presented before. The modelling of the circuits, as well as the verification of the circuits with the help of Avanwaves, both make use of HSPICE. The same individual is responsible for both of these procedures.

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