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Power Efficient and Energy Optimized Full Adder using GNRFET 32nm

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***Abstract*— This work investigates the output of a Full Adder constructed using XOR/XNOR gates circuit designed with FET devices, more specifically GNRFET, in 32nm. The work was proposed as part of a larger body of work. We adopt a complete adder circuit that utilises various logic types of XOR and XNOR layout, and we compare it to MOSFET-based circuits that have been used in the past. HSPICE simulations are utilised in order to investigate the product of a complete adder, and waveforms are verified. The terms power dissipation, delay, and power delay are all terms that are used to describe the amount of power that is dissipated and delayed. The purpose of this study is to determine which of the six GNRFET-based Full Adder Designs exhibits the highest output while simultaneously consuming the least amount of power and experiencing the shortest propagation delay in comparison to their counterparts. In contrast to current circuits, these circuits are designed to operate at a higher speed while using less power. It is likely that this will occur as a result of the low output capacitance. Each of the suggested complete adder circuits comes with its own individual set of benefits, both in terms of how much power they require and how quickly they add numbers. The HSPICE tool, operating in 32-nm technology, is used to carry out simulations for GNRFETs operating in the Shorted Gate Mode. In addition, the waveforms produced by the Avanwaves Waveform generator are used to validate the output of the complete adder circuits that have been proposed.**

Keywords—GNRFET; Low Power; Adder

I. INTRODUCTION

A substantial amount of electronic architectures is comprised of computerized circuitry such as microchips, highly specialized gadgets, and complex signal processors. If the scope of the reconciliation increases, the power and zone consumption processes will become a barrier to the convenience offered by circuits [1]. Because of the increased interest in and popularity of battery-powered multifunctional gadgets, designers are making an effort to reduce the resource consumption and territory of such frameworks as tablets, mobile phones, and workstations while maintaining their speed [2]. This is being done while still maintaining the speed of the devices. Increasing the W/L ratio of semiconductors is one method that may be utilised to decrease the power-delay of a circuit while avoiding the challenges that are generated by decreasing the stock voltage.

This tendency is responsible for the exponential growth in the number of processing systems that have been installed over the last several decades, since the reduction in transistor size has led to an increase in both the capability and complexity of devices [3]. However, the development of new technologies is hampered by scaling issues with silicon-based CMOS devices, and the ITRS has already forecast that Moore's law would be rendered obsolete within the next several years. Researchers might look at developing new methods and materials for the production of integrated circuits in order to further enhance the functionality of the device. Due to the imminent scaling limit, extensive research is being conducted on a wide range of innovative materials and technologies, including Germanium and Carbon in particular, as potential replacements for silicon. This research is being carried out since the scaling limit will soon be reached. [4-5]. As an example, one of the carbon nanotubes (CNTs), carbon allotropes that have been researched, and graphene have recently emerged as leading prospects for the replacement of silicon in post-CMOS technologies [6-9].

In many different applications, graphene is superior than silicon because of its superior carrier concentration, good thermal conductivity, and thin, planar structure. [10-

11]. This is as a result of its carrier's exceptional mobility. Graphene outperforms silicon in many applications [12-16] due to the fact that it is made up of a single atomic layer of carbon sheet that is structured in a honeycomb lattice. The movement of carriers in graphene is analogous to that of a massless particle; graphene exhibits both a high carrier velocity and an extremely high concentration of carriers. As a result of graphene's high thermal conductivity, it has emerged as a potential replacement for silicon-based devices in light of the difficulty associated with the removal of heat from densely packed silicon-based devices. Scaling of traditional silicon-based CMOS transistors has been much more difficult over the last several years for a number of reasons, including an increase in the wire resistance, a major decrease in mobility, and large dopant variations. Researchers are turning to a wide range of innovative transistor designs and materials in order to keep up with Moore's law, which states that computing power must increase exponentially every two years. Because graphene has such exceptional electrical and physical characteristics, the graphene nano-ribbon transistor, which is an electronic component, has attracted a lot of attention recently (GNRFET). The potential of the GNRFET in high-performance as well as low-power applications has been further underlined by early research that has been conducted in the theoretical, computational, and practical realms. In a number of different ways, the current-voltage (I-V) properties of the transistor are impacted by differences in the manufacturing process that occur in the transistor's size, oxide thickness, doping level, and peculiar graphene line edge defect. influence of substantial magnitude on the delay at the circuit level and the power efficiency. The challenges involved in the mass production of high-quality nanoscale graphene nano-ribbons raise more doubt on the commercial feasibility of this emerging technology (GNRs) [17]. The material must, among other things, widen an energy gap and shrink below 10 nm in order for GNRs to become semiconducting. This increases the difficulty of the manufacturing process. However, when CMOS technology is scaled down to nanoscale technology, short channel effects arise, which causes their I-V properties to deviate from those of normal MOSFETs. CMOS transistors, which stand for complementary metal oxide semiconductors, are the most commonly used transistors for the design of computer circuits. Because of this, alternative transistor technologies have been developed, such as the carbon nanotube field-effect transistor (CNT FET) and the graphene nanoribbon field-effect transistor (Graphene nanoribbon FET). CNT field-effect transistors (also known as CNT FETs) are one of the most promising technologies now available. These transistors have three terminals and perform tasks that are similar to those of MOSFETs. Carbon nanotubes make up this component, which serves the purpose of a semiconducting channel between the source terminals and the drain terminals. The development of graphene nano-ribbon field-effect transistors is providing more grounds for confidence over the future of technology. Graphene is used in the construction of this technique's semiconducting channel. Carbon nanotube field effect transistors (CNTFETs) are an exciting new nanoscaled technology that has the potential to construct exceptionally thick and low-power circuits at fast speeds and with a minimum amount of power usage. When a single carbon nanotube (CNT) or a group of carbon nanotubes are utilised as the channel material, as is the case in the traditional MOSFET design, the device is referred to as a Carbon Nanotube Field Effect Transistor (CNFET). A carbon nanotube serves as the functional heart of a CNTFET, which allows the device to operate in the correct manner. In this particular piece of work, the concept of CNTFET auditing is elaborated upon. The development, use, and properties of a large number of CNTFET variants have all been extensively discussed here in great depth. This research examines the job, dc, and execution characteristics of the CNTFETs, in addition to conducting an investigation of the manner in which a number of different quality measures are implemented [18]. A laser was used to transfer individual carbon nanotubes from an arrangement to oxidised silicon wafers that were equipped with gold or platinum terminals. The device that was created as a consequence was simple to fabricate and put into operation. Both the source and the drain functions were performed by the anodes, which were coupled with the nanotube channel. The gate function was provided by the doped Si substrate. FIG. 1.2 is a schematic illustration of this type of device, and it has been observed to clearly exhibit p-type transistor activity, with gate voltage control of the drain current beyond a few range requirements. Additionally, this type of device has been seen to clearly exhibit p-type transistor activity. Additional study showed that the devices had a high on-state blockage of several Low Trans conductance (- Ins) and no current immersion in MQ, which necessitated huge gate voltages in order to activate it. This was because there was no current immersion in MQ (a few volts).

In order to save money on power while simultaneously maximising the effectiveness of the data processing, As the use of battery-powered portable electronic devices like computers, tablets, notebooks, personal digital assistants, and personal networking systems (among many others) becomes more widespread, high-efficiency circuits (both in terms of the amount of power they consume and the amount of processing speed they achieve) are becoming an increasingly important component. Power consumption is an unavoidable aspect of VLSI systems [19]. There is a

direct correlation between the quantity of fuel that is wasted and the amount of heat that is taken from the apparatus. As a consequence of this, not only does the gadget's battery life decrease, but it also needs a more powerful fan in order to keep it cool. As a result of this, the device is guaranteed to become hotter. Because of this, the quantity of power that a system utilises has a direct bearing on the system's cost, weight, height, and the length of time the battery will last. On the other hand, when it comes to today's high-speed electronic applications, processing speed is of the utmost importance. Increasing the clock rate and the circuit density are both hampered by the amount of power that is used. A great number of VLSI implementations, to mention a few, have a significant amount of reliance on arithmetic operations, imaging, digital signal processing, and video processing, as well as microcontrollers and microprocessors. The four most popular arithmetic operations are addition, multiplication, subtraction, and the multiply and aggregate operations. Any of the aforementioned tasks might be accomplished with the help of the Extension function [12]. As a consequence of this, the performance of a 1-bit full adder cell is still an essential factor in determining the overall device efficiency metrics. In addition, a floating-point unit, the arithmetic logic array of the processor, and the generation of an address for a cache or memory entry all make use of a complete adder cell with a single bit of data. Using metal–oxide–semiconductor field effect transistor (MOSFET) technology, multiple complete adder cells with various logic types have been reported in articles up until now [20]. While each of these possibilities has both positives and negatives associated with it, it is important to note that there is no one optimal solution.

II. IMPLEMENTATION

Similar to Berkeley's SPICE-3, the analogue circuit simulator known as HSPICE enables users to conduct research in the frequency domain, transients, and steady states. It is not difficult to convert already-created SPICE decks for use with SPICE-3 to HSPICE, or to rebuild them so that they may take use of capabilities that were not available in SPICE-3. When compared to SPICE-3 and HSPICE, convergence is much better with the latter two. Due to the fact that it is a business product, support for it is superior (from Meta-Software). In addition to this, hierarchical node names, inputs, outputs, behavioural algebraics, and circuit optimization for parameterized cells, as well as waveform visualisation using MetaWaves that is interactive.

Running HSPICE to generate graph and hardcopy data files, followed by running MetaWaves to view, adjust, and print the resulting graphs, is the standard procedure for analysing a circuit. This procedure begins with the creation of an input file by using an editor (such as vi, emacs, or another similar programme). Beginning with an example input file and modifying it so that it fits the required circuit is often the easiest way to begin.

Producing a file known as an input netlist is a prerequisite for beginning the process of entering the design and simulating it. If you are just beginning started, you may want to put a sample file into your own personal directory and then modify the netlist to create your own circuit. This is something you can do if you want to. In order to get started with the analysis that is specified in the input file, enter hspice filename.hsp > filename.lis once the production of the file (filename.hsp) has been completed. In the event that the.option post is used, HSPICE will not only save the results of the desired simulation in an output listing file, but it will also save them in a graph data file. When post is supplied, the full circuit solution is recorded, whether it is in the frequency domain, the steady state domain, or the temporal domain. After then, the information may be analysed or visualised by utilising MetaWaves for any node voltage or branch current.

In order to start the analysis that is listed in the input file, you must add the options post and.end to a file that is being converted from the SPICE-3 format to the HSPICE format (make sure to press cr> after the.end statement to produce a full line). In the event that the.option post is used, HSPICE will not only save the results of the desired simulation in an output listing file, but it will also save them in a graph data file. When post is provided, the entire circuit solution is recorded, whether it be in the frequency domain, the steady state domain, or the temporal domain. After then, the information may be analysed or visualised by utilising MetaWaves for any node voltage or branch current.

It is only necessary to add the lines.option post and.end to a file that is being converted from SPICE-3 format to HSPICE format (make sure to press cr> after the.end statement to produce a full line). Adding the lines.option post and.end to a file is not required for any other purpose. In addition, HSPICE designates the function of each file through the application of specific file name patterns. All of the files that are associated with a particular design are stored in a single directory, and the names of those files are derived by concatenating the name of the design with a particular suffix. HSPICE and MetaWaves will first read the input file in order to determine the design name, and then they will use that name when creating the output files.

When implementing in VLSI back end using the Synopsys HSPICE software, it is essential to generate a circuit diagram complete with node numbers. After the node numbers have been added, an HSPICE netlist is

generated. Once the simulation is complete, various parameters, such as input and output waveforms, are analyzed. Calculations are done not only on power but also on latency and other aspects. These steps are repeated for each and every one of the circuits. 32 nm is the technological node methodology that is used for GNRFET.

The GNRFET used in the proposed study is operated in the shorted gate mode, which provides the best performance according to the parametric findings. Fig. 3 depicts the GNRFET-based circuit that was really used. In our recommended circuit, we employed two TG-based multiplexers, XOR gate, and two invertors to take complements of inputs as needed.

The gate of T2, T11, and the sources of T18, T8, T19, and T9 are all linked to input Cin. Input A is linked to the source of the T3 and T12 transistors, the gate of the T1, T10, T4, T13, and the source of the T16 transistor, while input B is connected to the source of the T4, T14, and T6 transistors. The transistors T17, T8, T19, and T6's gate are linked to the output of the XOR gate, while the transistors T7, T18, T9, and T16's gate are connected to the output of the XNOR gate, which is its complement.

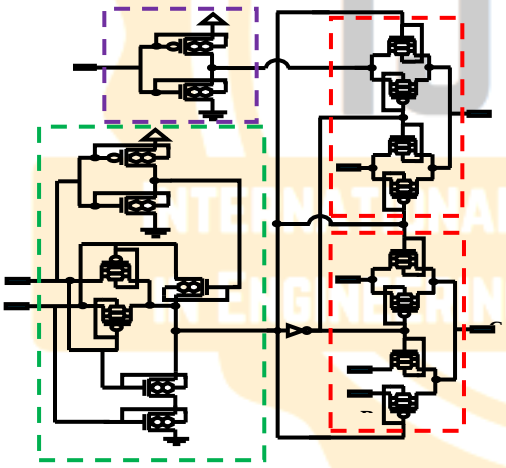

Fig. 1: Full Adder Circuit f using GNRFET (proposed)

The final suggested circuit for the full adder is shown in Fig. 1 above as the full adder circuit for Circuit f [1] utilising GNRFET.

III. RESULT

The outcomes for six circuits based on MOSFETs are illustrated in Fig. s2 to4. Of those, circuits b and f exhibit the best performance; as a result, they are taken into consideration for suggested circuits.

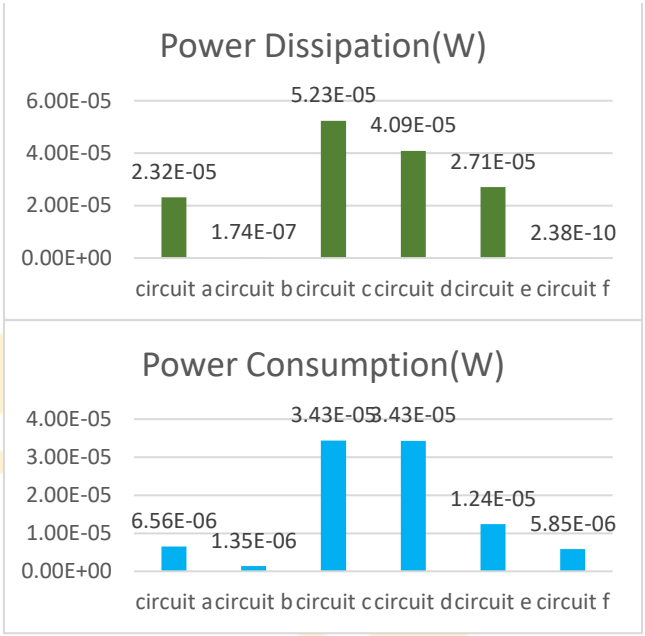

Fig. 2: Power Result (MOSFET)

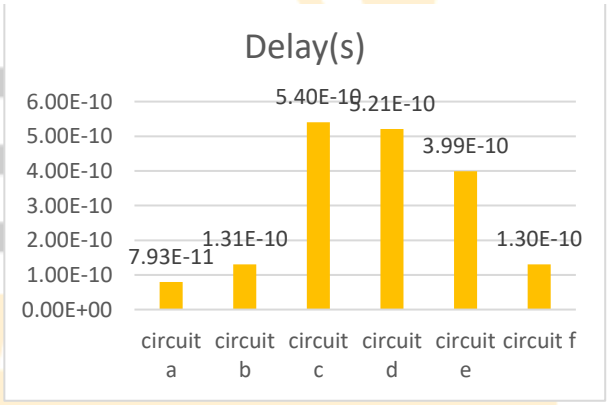

Fig. 3: Delay Result (MOSFET)

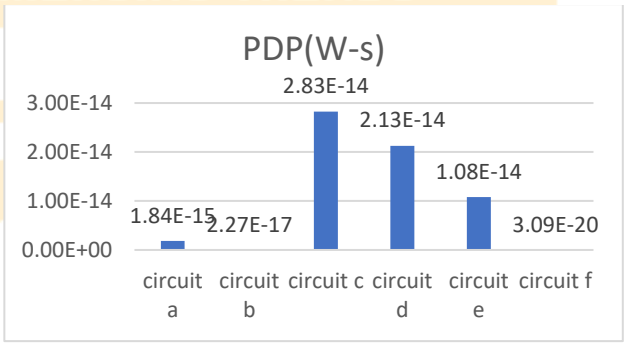

Fig. 4: PDP Result (MOSFET)

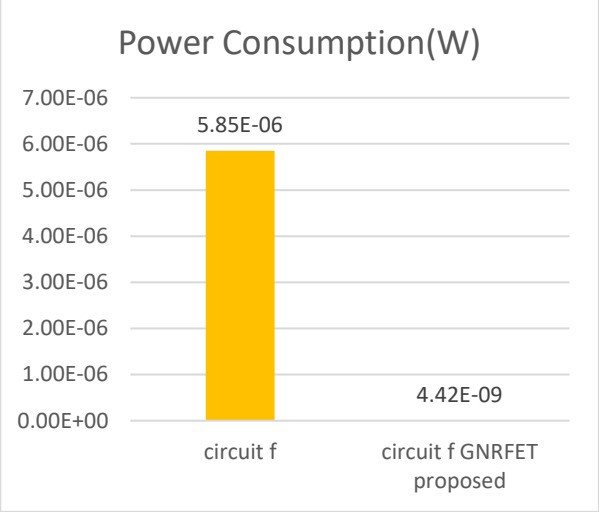

Fig. 5: Power Result (MOSFET Vs GNRFET)

In Fig. 5 to 8, circuit f proposed is compared with its counterpart and shows that they perform better in all circumstances. The graph above compares power consumption by MOSFET-based circuits with GNRFET-based circuits, and we discovered that utilizing GNRFET reduces power consumption by approximately 99% because of the scaling of the transistor node.

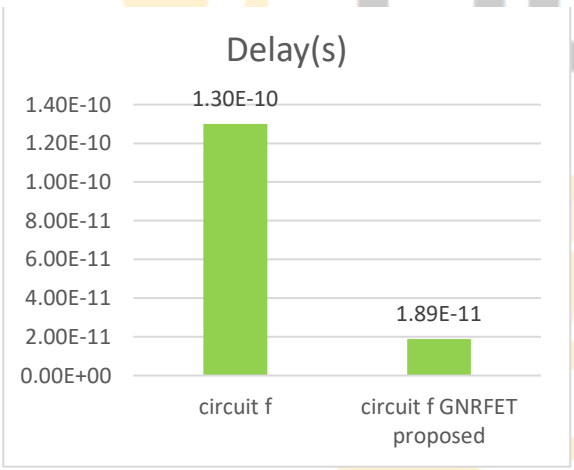

Fig. 6: Delay Result (MOSFET Vs GNRFET)

The graph above compares delay caused by MOSFET-based circuits to delay caused by GNRFET-based circuits, and we determined that using GNRFET decreases delay by around 85% due to high electron mobility and narrow band gap.

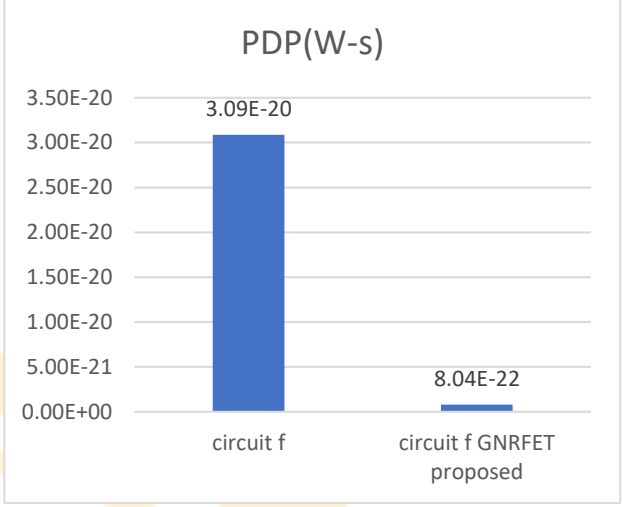

Fig. 7: PDP Result (MOSFET Vs GNRFET)

The graph above compares the power delay product generated by MOSFET-based circuits to the power delay product caused by GNRFET-based circuits, and we found that utilizing GNRFET reduces the power delay product by around 97% due to decreased power consumption and delay induced by circuits.

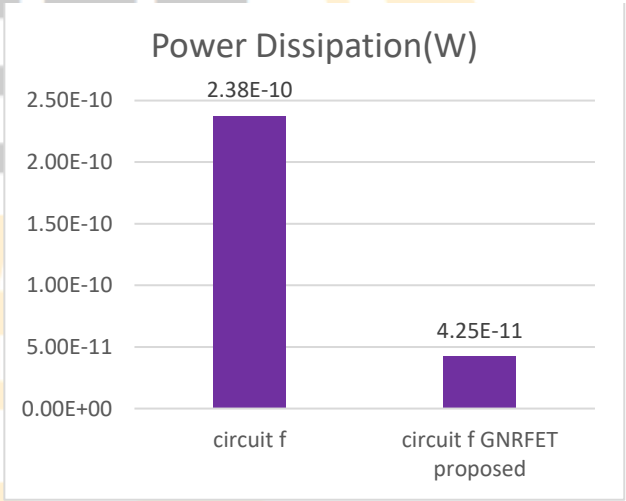

Fig. 8: Power Dissipation Result (MOSFET Vs GNRFET)

The graph above compares the power dissipation due to MOSFET-based circuits to the power dissipation due to GNRFET-based circuits, and we found that utilizing GNRFET reduces the power dissipation by around 82% due to less leakage power and high on and off current ratio.

In table1 and table2, the results are shown in tabulated form.

Table1: Result Table MOSFET based Adders

	circuit (a)	circuit (b)	circuit (c)	circuit (d)	circuit (e)	circuit (f)
Power Consumption (W)	6.56E-06	1.35E-06	3.43E-05	3.43E-05	1.24E-05	5.85E-06
Delay(s)	7.93E-11	1.31E-10	5.40E-10	5.21E-10	3.99E-10	1.30E-10
PDP(W-s)	1.84E-15	2.27E-17	2.83E-14	2.13E-14	1.08E-14	3.09E-20
Power Dissipation(W)	2.32E-05	1.74E-07	5.23E-05	4.09E-05	2.71E-05	2.38E-10

Table2: Result Comparison MOSFET Vs GNRFET based Adder

	MOSFET (adder)	GNRFET (adder)
Power Consumption(W)	5.85E-06	4.42E-09
Delay(s)	1.30E-10	1.89E-11
PDP(W-s)	3.09E-20	8.04E-22
Power Dissipation(W)	2.38E-10	4.25E-11

IV. CONCLUSION

The GNRFET model and HSPICE software are used to do a simulation on the described structure. HSPICE is software developed by Synopsys that is used for SPICE simulation. Because GNRFET libraries are compatible with this programme, it is highly recommended that you utilise it. Throughout the course of written history Because a full adder plays such an essential role in determining the output characteristics of a whole digital device, a number of different prototypes have been the subject of discussion. Each of these ideas has benefits and downsides, depending on how much power it uses and how quickly it operates. Either a dynamic or a static adder may make up the whole of a full adder. Although a dynamic style full adder has a smaller on-chip area and works more quickly than a static style full adder, it does have a number of intrinsic downsides, including a high clock load, charge sharing, poor noise immunity, and leakage. These problems may be found in both types of full adders. Finally, the power, PDP, and latency of both circuits are improved by the circuit that is presented, which makes use of GNRFET technology.

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