A Review on SRAM Using 7T FINFET Technology

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Abstract— The industry of integrated circuits (ICs) is still very much focused on getting its products to have the highest possible performance in terms of power consumption, delay, leakage, and time to market. This goal is still very much in the forefront of the industry's mind. Moore's Law, in its most fundamental expression, seeks to maximise the aforementioned qualities to the greatest potential that they are capable of doing by optimising them to their maximum potential. Gordon Moore, a well-known figure in the field of computer science, inspired the law's name. When the scaling of production nodes dropped below 32 nm, however, several tool settings became perilously close to approaching their limitations. It is noteworthy that one of the configurations, namely the power supply voltage, attained its maximum capacity. This is crucial because the power supply voltage is one of the settings that plays a big role in the generation of dynamic electricity. This limitation remained in place during the whole process of growth, despite the fact that it was still being applied. The objective of this study is to assess SRAM cells according to the amount of power that they generate.

Keywords—SRAM; Single Ended

I. INTRODUCTION

The memory capacity of System-on-a-Chip (SoC) designs is heavily influenced by the ever-increasing need for portable microprocessor-controlled devices like laptops, smartphones, and other communication devices. In particular, developments in mobile computing have spurred this desire. To increase the useful life of these portable devices, it is crucial to lower the power consumption of their circuits. Low power consumption can be achieved by unconventional device designs, novel circuit topologies, and architectural optimisations.

Some aspects of circuit design, most notably the voltage supplied by the power supply, were unable to undergo additional reductions throughout the process of scaling down manufacturing nodes to below 32 nanometers. Despite ongoing efforts to scale, this limitation affects the flexibility of power usage.

SRAM, which stands for "static random-access memory," is a crucial type of memory used by computers. Unlike magnetic tapes and drum memory, SRAM allows data objects to be read from and written to with the same access time regardless of their physical locations inside the memory device. As opposed to other forms of data storage, such magnetic tapes, this has several advantages. SRAM's random-access characteristic provides this advantage since it is far more efficient than traditional data storage medium with direct access that is limited by mechanical limits.

In order to execute read/write operations, the SRAM memory chip incorporates multiplexing and demultiplexing circuitry. It is common for SRAM devices to include several data lines, with the amount of bits being labelled as "8-bit" or "16-bit" depending on the total number of lines. RAM, which includes SRAM, is commonly linked with volatile memory types like DRAM due to its widespread use in a wide range of electronic devices. SRAM may be used to implement RAM as well. The advent of non-volatile RAM, on the other hand, has increased the scope of what may be stored in a computer's RAM.

Embedded memory is an integral aspect of the design of microprocessor-controlled devices, especially system-on-a-chips (SoCs). For the battery life of these devices to be prolonged, low-power circuits are required. To achieve this goal, it will be necessary to employ novel device architectures, alternative circuit topologies, and technical advances. Using the common 7T cell, scaling the voltage for ultralow power operation presents a number of challenges.

Static random-access memory (SRAM) is a kind of RAM that has become popular because to its lightning-fast access

speeds and total lack of data refreshing requirements. Because of this, a lot of effort has been put into optimising it so that it can meet the need for high-capacity memory in a space that would otherwise be too small to accommodate it. Thanks to advances in computing and connectivity, SRAM is now used in satellite navigation and driverless automobiles. As a result, there has been a dramatic expansion in the amount of information that can be accessed rapidly.

Memory technologies including dynamic random access memory (DRAM), static random access memory (SRAM), non-volatile static memory (NVSM), and flash random access memory (FLASH) have proliferated in recent years. These memories are crucial to the growth of the electronics industry as a whole, since they are used in everything from personal computers and mobile phones to computer networks and other related electronic devices. SRAM has quickly risen to prominence as one of the most widely used forms of memory because to its combination of small form factor, large storage capacity, rapid speed, and exceptional dependability.

Because of their limited capacity, SRAM cells must strictly adhere to a set of static characteristics to ensure the reliability of the data they store. The Static Noise Margin (SNM) can be used to measure the reliability of data stored in SRAM cells. When there is some DC noise present, the SNM indicates that the steady-state data state of the cell may be disrupted. To ensure proper functioning even in the face of noise signals or other interruptions, it is crucial to design SRAM cells with a high level of stability.

In order to meet the ever-increasing need for data storage, manufacturers have evolved their methods in accordance with Moore's Law, allowing for a greater density of transistors per chip. High-performance memory circuits that are also compatible with current system-on-a-chip (SoC) technologies are crucial. Memory's value stems from the fact that it does more than just store data; it also facilitates reading, writing, and retrieval. SRAM is a type of volatile memory, as opposed to nonvolatile memory, which has other applications.

Laptops and mobile phones, which rely on batteries, are becoming increasingly common, thus manufacturers are working to reduce the static power dissipation rate. Since cache memory occupies a sizable portion of a SoC, great care must be taken to minimise power loss caused by leakage in SRAM. When compared to dynamic random-access memory (DRAM), static RAM (SRAM) is faster and uses less energy. This demonstrates its potential for serving as a temporary data storage medium. SRAM's great responsiveness and low power consumption demands make it a potential replacement for DRAM in low-power devices.

II. Literature Review

Previous research on FinFET static random access memory (SRAM) examined the potential benefits of using FinFET technology rather than traditional MOSFETs in terms of performance, power, and stability. The use of FinFETs in SRAM design has been the subject of a great deal of research [1, 2, 3].

Static noise margin (SNM) improvement is an important area of study since it affects the reliability of SRAM cells. Increased leakage current control shown by FinFETs mitigates the effect of various noise sources. FinFET-based SRAM cells have a larger SNM than MOSFET-based cells, leading to better data retention and stability. Research [1] supports these findings.

There is also some indication that FinFET technology can assist address process unpredictability and variance. Better electrostatic control and more stringent management of short-channel effects make FinFETs more forgiving of manufacturing imperfections [2]. This quality is very helpful in the creation of SRAM, where it is necessary to match transistors precisely to ensure the flawless execution of read and write operations.

Researchers have also looked into how FinFETs affect power consumption in SRAM layouts. Leakage current is a significant contributor to the overall power dissipation that SRAM cells are responsible for, and it has been shown that FinFETs (Fig. 1) have a lesser leakage current than MOSFETs. FinFET-based SRAM cells have been shown to be more energy-efficient due to their lower power consumption at rest [3, 4].

The read/write and access timings of FinFET-based SRAMs have also been investigated. These tests and investigations have already been done. Higher operating speeds can be achieved with FinFETs [1] due to better management of short-channel effects and lower parasitic capacitances. This gain has implications for memory-intensive high-performance software.

FinFET static random access memory (SRAM) has been shown effective in previous research. Possible performance improvements are investigated while the static noise margin is increased, process fluctuations are decreased, energy consumption is lowered, and more. These results have contributed to the study and optimisation of FinFET-based SRAM designs that is still underway. These efforts are being undertaken with the eventual goal of increasing the efficiency

and dependability of SRAM memory arrays used in cutting-edge semiconductor technology.
One of the most interesting topics of study is the stability of FinFET SRAM under various operating circumstances. FinFET-based SRAM cells' dependability and consistency in the face of temperature, process, and supply voltage fluctuations have been investigated in [4] and [5]. Even while functioning in less-than-ideal settings, the SRAM must continue to perform its intended functions and safeguard the integrity of the data it stores.

To further improve FinFET SRAM's performance, scientists have investigated a plethora of cutting-edge circuit approaches and design methodologies. Read/write performance, energy efficiency, and robustness to process disturbances may be enhanced with techniques such as body-biasing, adaptive voltage scaling, and assist methods [6][7]. These goals can be achieved by the implementation of the following strategies, which have been assessed for their efficacy.

There has also been a lot of focus on the scalability of FinFET SRAM. Increasing density while decreasing feature size is becoming increasingly important in the semiconductor industry. The potential of scaling FinFET-based SRAM cells to sub-10 nm technology nodes has been investigated by scientists [8, 9]. To prove that FinFET SRAM may be used in subsequent generations of technology, experiments were performed to measure how scaling affects critical performance measures including access time, power consumption, and stability.

Possible sources of FinFET SRAM reliability difficulties, including as ageing effects and soft mistakes, have also been extensively researched. Studies [10] and [11] looked at the effects of ageing on the long-term stability and performance of FinFET-based SRAM cells. Some of these consequences include TDDB (time-dependent dielectric breakdown) and NBTI (negative bias temperature instability). Researchers have investigated the vulnerability of FinFET SRAM to radiation-induced soft errors [12], [13] to assure the lifespan of the memory cells in high-radiation environments.

Current studies on FinFET SRAM have covered a wide range of topics, including stability analysis, circuit approaches, scaling concerns, and reliability hurdles. Researchers believe that by concentrating on these aspects, the full potential of FinFET technology in SRAM designs may be realised, resulting in high-performance, low-power, and long-lasting memory solutions in state-of-the-art semiconductor technologies.

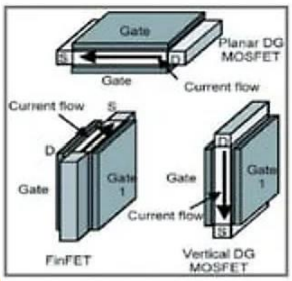

Fig. 1 FinFET [8]

III. CONCLUSION

The choice taken at the outset of the integrated circuit industry to optimise for overall performance, power, delay, leakage, and time to market (opportunity cost) has not changed, regardless of any advances in technology. Despite developments in technology, this option was still chosen. The advancements in technology have not stopped this decision from being made. This choice was selected to provide the highest quality of results from these measurements. In reality, Moore's rule is based on the concept that the value of such traits should be raised to the greatest extent feasible. Despite the fact that key tool parameters could no longer be adjusted, production node scaling continued in the direction of 32 nanometers. Despite the fact that scaling was no longer an option, this was executed. This was notably true with respect to the voltage of the power source, the single most important factor in the production of kinetic energy. This review gives idea on SRAM based on FINFET.

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