International Journal for Research in Engineering and Emerging Trends (IJREET), Volume 7, Issue 1, March, 2023
ISSN: 2545-4523 (Online)

A Review on Low Power Optimized 14t SRAM Cell for Space Applications using FinFET in Trigate Mode

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Abstract:

In this paper, which is about an SRAM cell review on aerospace technology, we try to collect some research for a novel radiation-hardened 14-transistor SRAM bitcell that is speed and power optimised [(RSP)-14T full form can be described as radiation-hardened with respect to speed, power optimised] for the space application, which is proposed. [RSP] stands for radiation-hardened with respect to speed, and power optimised. The findings of the mixed-mode simulation reveal that the innovative structure has enhanced resistance to single tone-event upsets as well as single-event n multiple-node upsets. This is because the novel structure provides more redundancy. This is due to charge sharing by OFF-transistors, which was created in this 65-nm CMOS method via circuit- and layout-level optimization and design. The reason for this is because charge sharing by OFF-transistors was developed. In addition, the findings from our HSPICE simulations demonstrate that the write speed and power consumption of the proposed RSP-14T memory cell are increased by approximately 65% and 50%, respectively, when contrasted with those of the radiation hardened design (RHD)-12T memory cell. This is the case when comparing the two.

Keywords: *High speed, low power, radiation-hardened SRAM, single-event–multiple-node upsets (SEMNUs), single-event upset (SEU).*

Introduction:

SINGLE-event upset, sometimes referred to as SEU and commonly abbreviated as "SEU," is a kind of single-event effect that is non-destructive and falls under the umbrella term "soft mistake" [1]. Ionization of a particle takes happen when the particle is subjected to radiation and a heavy ion collides with a substance that is composed of a semiconductor. Because of this, the particle is subjected to the circumstances that are required for ionisation. These extra charges are going to be collected by the nodes of the device, which are very sensitive to their surroundings. Because of this, a voltage disturbance will show up at the nodes that are vulnerable to it as a

direct result of what has happened. When the amplitude of the voltage disturbance in an SRAM bit cell is sufficiently high and above the logic threshold level of the inverter, there is a possibility that the data that has been stored will be inverted, which is another way of stating that a SEU will be produced.

As a result of the unceasing development of CMOS technology, the minimum spacing that must be maintained between transistors is now in the process of being reduced.

Because of this, a higher number of transistors are vulnerable to the charge that is deposited by a single particle hit [2], in contrast to the approaches that came before, in which only a single transistor was in use. The sharing of a charge leads in single-event–multiple-node upsets (SEMNUs), which are progressively becoming the principal effect of energetic particle striking in forthcoming nanometer-scale CMOS technology [3, 4]. In addition to this, reducing the supply voltage considerably increases the likelihood that the circuits will be negatively affected by the impacts of radiation. Because of this, there is an unquestionable need for the study and development of technologies that can tolerate radiation in digital circuits [5]. Because of its substantially higher sensitive volume per bit and lower node capacitance, SRAM is more prone to soft errors than its dynamic counterpart. This is because SRAM has a lower node capacitance. This combination renders SRAM more susceptible to errors than it would be otherwise. Due of this, the soft error rate (SER) [6] in SRAM is also improved as technology advances in the nano-metre zone. [Citation needed] In order to bring down the SER, numerous additional potential substitutes for the quality standard 6T SRAM cell have been offered [7–15]. These replacements may be found in a variety of different types. The major method of increasing boost is performed by the creation of a one-of-a-kind topology for the connecting of transistors inside cells. This topology's primary purpose is to provide protection at the circuit level. A soft error aggressive Quatro-10T SRAM cell was described in reference number [7], which may be found here. This cell has a large noise margin and is capable of performing a wide range of read operations. Sadly, it can only recover from "1" to "0," which means that due to this constraint, it cannot completely protect against SEU. Because to the feedback from the dual node, the dual interlocked storage cell (DICE) [8] may be completely immune to the effects of a single-event transient (SET) if it occurs on either of its single nodes. Despite this, there is still a need for improvements to be made to the fundamental capabilities of SEMNU's immunity and radiation hardness performance. The Schmitt trigger was used in the manufacturing of the Schmitt trigger based (STB)-13T memory cell that had 100% immunity to SEU. This memory cell was detailed in reference (4). However, in order to obtain the limited enhancement of SEMNU's immune potential, it is necessary to make a sacrifice in terms of writing speed, increase the amount of power that is used, and increase the size of the layout area in comparison to DICE. Only then will it be possible to gain access to the restricted enhancement. The STB13T served as the foundation for the creation of two new kinds of radiation-hardened memory cells, which were given the designations RHD-11T and RHD-13T [9]. These cells have a greater degree of dependability than the cells that came before them. However, throughout the course of time, both

their writing speed and their write margin have been worse. For radiation-hardened applications that need low power consumption and a high level of reliability, the RH memory (RHM)-12T was also demonstrated in [10]. Nevertheless, the pull-up device that the designers used was a nMOS transistor, which led to insufficient read noise margins. This was a significant oversight on their part. Recently, a memory cell with radiation hardness and performance that are to the user's liking was published in [12]. This cell is called as the RHD-12T, and it can be seen in Fig. 2 that both of these characteristics are to the user's liking (a). In addition to the possibility that any of its internal single nodes may be affected by a SEU, it also has the capacity to provide the SEMNUs with some level of protection to the condition. However, the restricted application of apps for it is owing, in large part, to the slow writing speed as well as the higher power consumption. Both of these factors have contributed to the limited success of application development. It has also been suggested that certain designing techniques may be used as an extra tactic for increasing radiation tolerance [13], [14]. In addition to the upgrade that has been included at the circuit level, these strategies have also been employed. Based to the results presented in [13], a novel layout approach known as layout design utilising error-aware transistor placement (LEAP) was applied to DICE. This resulted in the construction of a new subsequent element that was given the name LEAP-DICE. [13] According to the findings of the TCAD simulations, it was effective in increasing the threshold at which the linear energy transfer (LET) started to become disruptive. As a method for carrying out the charge sharing test, the author of reference [14] provided a Monte Carlo simulation platform that was given the name "Tool suite for radiation reliability assessment" (TIARA). The layout optimization of the transistor pairs that are most likely to create difficulties may be achieved within the scope of the objective if the results of the TIARA simulations are analysed and analysed thoroughly. The topic of the current research project and the proposal for it is the radiation-resistant, speed- and power-optimized (RSP)-14T bitcell. Its radiation hardness has been substantially improved in comparison to RHD-12T as a result of the building of more nodes, each of which comprises two more pMOS transistors. This was accomplished owing to the inclusion of the nodes. During the write operation, the feedback mechanism will be disturbed more often due to the fact that an extra PMOS is controlling the supply of the branch that contains the redundant nodes. This is because the branch is being controlled by an additional PMOS. As a direct consequence of this, there has been a considerable increase in both the write speed and the power usage. SPICE simulations utilising the double-exponential current source model are often used for the purpose of testing the radiation tolerance of the circuit. This allows for a considerable decrease in the amount of time spent on the procedure. Nonetheless, the accuracy of the model is based on calibration criteria that are not based in the actual world. Since there is no charge sharing between the transistors, it is feasible that the SEU immune capacities of other SRAM cells will be overestimated [16]. This might happen as a consequence of the lack of charge sharing. This research makes use of TCAD mixed-mode simulation, which is an effective qualitative method for analysing SEU immunity. It is used because it enables the inclusion of charge sharing between transistors while simultaneously lowering the burden placed on the CPU. The findings

of the simulation, when considered in combination with the design at the layout level, demonstrate that the newly included circuitry has much increased SEU immunity. The circuit under study is shown in Figure 1.

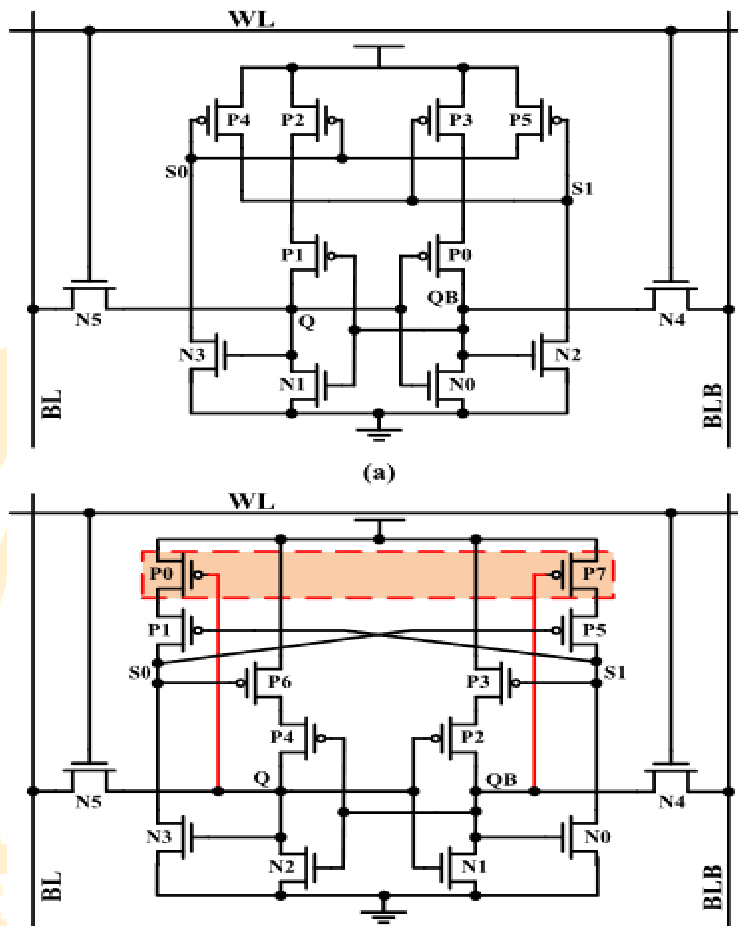

Figure 1: SRAM 14 Cell

Review of Previous Work:

Following the enhanced performance and area advantages, as the appearance of a non-planar CMOS devices at this 22-nm node and above, it is extremely likely that a multi-gate device adaptation will take place in a superior and high-performance the process technology. This is because it is extremely likely that a multi-gate device adaptation will take place in a superior and high-performance the process technology. In this study, we compare symmetric (Symm-G) and asymmetric (Asymm-G) gate work function FinFETs in a high-performance process using technology computer-aided design 3-D device simulations. We find that symmetric gate work function FinFETs perform better than their asymmetric counterparts. This comparison has never before been made and is being done so for the very first time now. We demonstrate that as

Asym-G shorted-gate (the a-SG) n/p-FinFETs, which use as both work functions as corresponding to the typical as high-performance metal-gate n/p-FinFETs, are such promising devices, as if they can yield over two orders of magnitude lower or lesser leakage in lacking excessively degradation at ON-state current, in comparison to Sym-G SG (shorted-gate) FinFE Following that, we may examine the design space of FinFET logic gates, latches, and flip-flops using mixed-mode 2-D device simulations in order to find the ideal tradeoffs in leakage vs the latency and the temperature. By exploring the design space of FinFET logic gates, latches, and flip-flops, one may find the best tradeoffs for a given set of requirements. The elementary logic gates that make use of the Asym-G the SG-mode FinFETs appear to be located optimally in this the leakage–delay spectrum, in comparison to the most versatile configurations that are possible by mixing corresponding Sym-G SG- and IG-mode FinFETs. These gates are named as shown INV, the NAND2, the NOR2, the XOR2, and the XNOR2. Nevertheless, in order to maximise leakage, delay, and setup time all at the same time, latches and flip-flops need a skillful combination of Sym-G and Asym-G FinFETs. [2]

In the work that has been offered, a viewpoint and an analysis for FinFET devices have been provided. These devices have been examined with the major emphasis being focused on the sub-threshold leakage current control. In order to realise this objective, it will be essential to develop asymmetric work functions for the four terminal FinFET devices, in addition to correctly biassing the back gate. In addition to this, we are researching the many different configurations of multiplexers and XOR gates that are feasible by using transistors that have both symmetric and asymmetric work functions in their designs. As compared to the findings that were discovered in the published research, the configuration that we presented, which used symmetric devices, resulted to improvements in leakage current and delay of roughly 65% and approximately 47%, respectively. The substantial characterization data that was gathered for the MUX circuits served as the foundation for this enhancement. It is feasible to acquire an improvement of about 90 percent in the average leakage current for the XOR gates by making use of asymmetric devices. This is easy to do. Every simulation was carried out using the UFDG model that was developed by the University of Florida. This model is predicated on a 25nm FinFET technology. [3] The goal of this study is to reduce the amount of space and power that is needed by a 2:1 multiplexer (MUX) while maintaining its performance at a level that is comparable to that of other similar devices. In the design of the various configurations, many topologies of 2:1 MUX are used. Some examples of these topologies include CMOS-based MUX, transmission gate and pass transistor utilising n-shaped field e®ect transistor, and others (FINFET). The mobility of the devices with longer ns was greatly enhanced because to the greater tensile stress that was applied to them. When applied to DG, FINFET has the potential to be employed efficiently to enhance performance while simultaneously minimising the amount of power that is used. When linking together parallel transistors, one of the available options for controlling noncritical channels is to make use of self-determining gate control. We have computed the optimal power, the optimal current, the leakage power, the leakage current, the operating power, the operating current, and the delay in a voltage supply of 0.7 V at a variety of

temperatures, including 10 degrees Celsius, 27 degrees Celsius, and 50 degrees Celsius, respectively. Using 45 nm CMOS process technology, an access time of 20 ns and a frequency of 0.5 GHz are supplied in order to carry out a new architecture of 2:1 MUX utilising FINFET. This is done so that the architecture may be carried out. In addition, the voltage utilised for the power supply is 0.7 V. [4]

The double-gate FinFET is a one-of-a-kind device structure that is used in the nanoscale domain. This is because, in this regime, the performance of conventional CMOS technology begins to decline owing to excess short channel effects. The reason behind this is because FinFET is used in the nanoscale regime (SCEs). The performance of regular FinFETs is not nearly as excellent as that of double-gate (DG) FinFETs, which helps with the scalability of the technology. This is in comparison to the performance of traditional CMOS. Within the scope of this investigation, we are developing 32-nanometer DGFinFETs and evaluating the characteristics of these devices with the assistance of Sentaurus TCAD. The results of the device's simulations indicate that it is feasible for it to be controlled on a scale that is nanometer-level or smaller. The DGFinFET has gates that are entirely distinct from one another, and the threshold voltage of any gate may be customised by modifying the voltage at another gate in the device. When this phenomenon is used, a logic circuit has the potential to be configured to function in any one of the following modes: SG mode, LP mode, IG mode, and IG/LP mode. The node that was just mentioned includes the building of both an INVERTER and a NAND gate, and a comparison between the two of these components has been made. The results of the simulations indicate that the SG-mode configuration is more than enough for high performance design. [5]

The usage of a model that is founded on physical principles is required in order to check for shortchannel effects (SCEs) in undoped nanoscale self-dependent-gate FinFETs like the MIGFET. One such model is described in the following sentence (L. Mathew, et al., Proc. IEEE Internat. SOI Conf., p. 187, 2004). The threshold-voltage rolloff, subthreshold-swing deterioration, and drain-induced barrier lowering are actually less severe in this configuration of the device than they are in the double-gate mode, as anticipated from the current–voltage characteristics of MIGFETs operating in the single-gate mode. The results are now being provided with explanations that are not only understandable but also insightful. [6] Because of the scaling down of this technology, there is a growing focus put on the relevance of power analysis and leakage current in the memory architecture. The authors of this work discovered a superior choice for the low power connection as synthesis at the 45nm node and beyond this using Fin-type Field-Effect Transistors (the FinFETs), which are a prospective alternative for the bulk CMOS at the gate lengths that were studied. This was accomplished by using the FinFETs, which are a type of field-effect transistor that is shaped like a fin. We take into account a strategy that is known as variable-supply voltage schemes, which is intended to improve the performance of FinFETs by enhancing their efficiency. Since there is no body effect, it is common known that minimising leakage in double-gate technologies such as FinFETs by stacking transistors does not work very well. This is because there is no body effect. The absence of a bodily effect is the

cause of this phenomenon. Nonetheless, transistor stacking, in combination with the variable supply voltage behaviour of FinFETs, may give rise to larger leakage reductions than bulk devices. The reference paper that follows provides an example of an excellent design and implementation of a FinFET-based 4x4 size SRAM cell array, which can also be understood as a one-bit 7T SRAM. The leakage current, the dynamic power, and the latency have all been analysed for the FinFET based on the 7T SRAM, and all have been found to be consistent with what was anticipated. The fabrication of the FinFET device has been carried out precisely according to the design that was envisioned. After that phase, a 2:4 decoder was built, and the results that were obtained by the recommended model were double-checked to ensure that they were accurate. The output of a FinFET SRAM array was compared with the output of a conventional CMOS SRAM in order to validate our design technique. As a consequence of this comparison, significant improvements were realised in the recommended model, which led to the validation of our design process. [7]

MOS is one of the older technologies for transistors, and despite the fact that it has the benefit of having a low power consumption, it also has a shorter channel for the flow of current. As a consequence, it has certain drawbacks, such as having a larger size and the requirement to use current that is not necessary. The channel gate of a new device that is being developed and is known as the FinFET (Fin Field Effective Transistor) is much longer. After starting off at 32nm by Intel and then being lowered to 14nm by Samsung, the size may be as low as 14nm by Samsung. This comes after Intel's initial size of 32nm. This project's study will centre on two technologies: CMOS and FinFET, as well as the techniques by which we can discriminate between the two and raise the value of CMOS. The research will also concentrate on the methods by which we can increase the value of CMOS. [8]

The whole set of 16 functions has been broken down in a brand new fashion, and a brand new circuit design for re-configurable dynamic logics with two inputs that is based on double-gate MOSFETs has been produced. Both of these developments have been made possible by the discovery of double-gate MOSFETs. A 16 function 12T DRDLC with two states of control gate voltages (+V, 0) and a 14 function DRDLC with two states of control gate voltages (both 0 and -V) have recently been accessible to the public. Both of these DRDLCs feature two states of control gate voltages. By merging these two examples, each of which utilises a state control gate, it was possible to effectively produce the 12T DRDLC with three different states of control gate voltages (+V, 0V, and -V). Newly proposed DG-MOSFETs having two states, such as (+V, 0) and (0, -V), may often be efficiently realised using the presently existing OR type and AND type IDG-MOSFET. The newly proposed circuit architecture may be one of the most promising choices for the ultimate realisation of re-configurable LSIs in the future. In particular, this holds true for the 16 functions 12T DRDLC scenario with two states (+V, 0). [9]

Since it has two gates that may be controlled as independently as possible, the FinFET, which we use in a double-gate field effect transistor (the DGFET), is more flexible than traditional single-gate field effect transistors. This is due to the fact that the FinFET has two gates. The fact that

the FinFET has two gates is the explanation for this behaviour. The threshold voltage of a FinFET transistor's first gate may typically be dynamically regulated by the usage of the second gate of the transistor, which is the case in the majority of instances. This is done in order to improve the performance of the transistor as well as reduce the amount of power that is lost due to the transistor's leakage. After this, we will be able to create circuits with a reduced total number of transistors by making advantage of the FinFET's second gate as well. In other words, we will be able to design circuits that are more efficient. That is due to the fact that one of the key considerations that went into the design of this circuit was making efficient use of the available space. Both of these gates of FinFET transistors were used as inputs in the presentation of the article that illustrated a novel method for constructing the majority gate and the 2-1 MUX. This method was displayed as part of the presentation. The reference paper that was delivered included extensive explanations of this method. The findings of the simulation indicate that the implementation of FinFET logic offers a significant benefit over the implementation of static CMOS logic and pass transistor logic in terms of the quantity of power that is used and the size of the cell that is required to house it. [10]

The fundamental objective of this study is to present and assess a comparative performance study of low-power FINFET-based diverse designs of XOR and XNOR circuits. This will be done by comparing and contrasting the results of each design. Using this article as a means to reach this goal will bring about the desired results. When scaling typical CMOS circuits, the short channel effect often occurs as a consequence of increases in the amount of leakage current that occurs inside the circuit. The use of FINFET, rather than the more conventional CMOS circuits, could be able to assist alleviate the adverse impacts of short channels. During the duration of this essay, we are going to conduct an in-depth analysis and comparison of the performance of XOR and XNOR logic circuits. A comparison of numerous different design methodologies for XOR and XNOR logic circuits is going to be carried out so that the results may be analysed and compared. The CADANCE VIRTUOSO tool is used in order to evaluate the functionality of XOR and XNOR circuits. When the temperature is set to 270 degrees Celsius, the voltage supply is set to 0.7 volts, and all of the simulation outputs have been created using the Cadence SPECTRE simulator utilising 45 nanometer technology, the conditions for this simulation are as follows: The XOR and XNOR circuits, in addition to designs that incorporate a static circuit, transmission gate, and feedback transistors, are the ones that work the best for arithmetic circuits. Other designs that perform well include: The findings of the simulation indicate a moderate degree of dynamic power consumption and a low quantity of power, delay, power, delay product (PDP).. [11]

Conclusions

Hence, this study presented that covered the literature review for the radiation-hardened 14T SRAM bitcell with the speed and the power optimised (the RSP-14T). This bitcell was based on the source isolation approach that was reviewed and presented in this article. For as the circuit- and the layout-level optimization, you can use the mixed-mode simulation previous work show

that it cannot also tolerate a SEU on any of its inner single node, but also having the partial SEMNUs immune even at the LET value equal to 60 MeV-cm2/mg, which is larger than what has been reported for RHD-12T. This is because the LET value is determined by the amount of energy transferred per unit area. In the meanwhile, as compared to the RHD 12T, both its write speed and the amount of power that it consumes have seen considerable improvements. As a result, the accepting area was somewhat expanded, and the planned RSP-14T cell is more suited for use in space.

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