14T SRAM Bit cell with Speed and Power Optimized using Shorted Gate FinFET

Akanshi Singhal
M.Tech Student.
Dept. Electronics & Communication Engineering
S.D. College of Engineering & Technology.

Er. Parul Gupta
Professor
Dept. Electronics & Communication Engineering
S.D College of Engineering & Technology.

ABSTRACT: The tendency to maximize performance measures such as overall performance, power, delay, leakage, and time to market (opportunity cost) has not altered because of the development of the integrated circuit industry. In point of fact, Moore's law is all about finding the optimal values for those parameters. Unfortunately, when the scaling of generating nodes moved closer and closer to 32 nm, several of the tool parameters were unable to be scaled any further. This was especially true for the power supply voltage, which is the primary component in determining dynamic electricity. The purpose of this study is to find ways to reduce the amount of power used, as well as delays and leakage currents in 14T SRAM cells. For the purpose of determining both the power consumption and the latency of the SRAM, the backend device Synopsys HSPICE was used. This study designs and simulates a 14T SRAM in the era of 22 nm using SG-FINFET technology. The simulations are carried out in 22 nm.

Keywords: High speed, low power, radiation-hardened SRAM, SRAM Cell, FinFET, CMOS, delay.

1. INTRODUCTION

Because of advancements in nanoscale process technologies, chip densities and operating frequencies have increased. This has resulted in increased energy consumption in battery-operated portable devices, which is a primary problem. Even for non-portable electronic equipment, adequate power consumption is essential because of the increased costs associated with better packaging and cooling, in addition to concerns over ability dependability. Therefore, the major basic design objective for the VLSI (very-large-scale integration) designers is to meet and match total performance as this task required within our power budget. This is because VLSI is an acronym for very large-scale integration. [3] Scaling of gate MOSFET in nm faces an extraordinary assignment because to the very short channel effect, which causes an exponential development in the sub-threshold and gate–oxide leakage as well as the DIBL. [1]. In the nanoscale, FINFET is an attractive replacement for bulk MOS because the fabrication method for FINFET and MOSFET is essentially the same [2]. FinFET (fin-type DGFET)[4] offers an interesting strength–delay tradeoff and higher characteristics (as short channel effect) in the form of a nanometer, both of which will be meet to the overall performance as we expected it to be through exploring global technology for the semiconductor for this drawing close technological node. [5].

The FinFET is a kind of significant steel oxide semiconductor field effect transistor/MOSFET. This classification was given to it because of its influence on these devices. It was Channing Hu and his colleagues at the University of California, Berkeley, who made the first advancements in the concept. The NMOS in CMOS technology is replaced with N-FinFET in FinFET, and the PMOS is replaced with P-FinFET in FinFET. Both gates of FinFET are then collectively coupled together. [7] With the assistance of the utilisation of this strategy, we will lay out a FinFET model of a CMOS common sense circuit or a bypass transistor good judgement circuit. This circuit will maintain identical functions as the MOSFET model. [6] FinFET gives greater circuit performances and minimises leakage current day by effectively suppressing the quick-channel effect and providing near-best sub-threshold swing [9]. This occurs throughout the span of time in between the two previous statements. The FinFET Device is shown in Figure 1. [1] A single-event upset, also known as SEU, is a software fault and a nondestructive kind of single event effects, often known as SEEs. It is possible for the particles to get ionised in an environment containing radiation if the heavy ions are impacted on the semiconductor material at the same time. Because of the sensitive nature of the nodes that make up the device, these additional or supplemental charges may build..

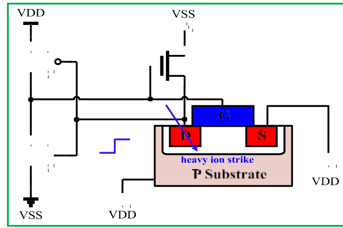

Fig.1: SEU induced by an ion strike in an SRAM memory

In addition, lowering the supply voltage any more will make circuits more vulnerable to the effects of radiation in a manner that is quite similar. Because of this, the development of radiation-resistant technology that may be used in digital or virtual circuits is of the utmost importance [5]. SRAM is more susceptible to software mistakes than its dynamic cousin due to the bigger sensitive volume for each bit as well as the lower node capacitance. As a result, the number of soft errors that occur in SRAM increases at a faster rate (SER) [6] as the generation is scaled withinside the nanoscale range. In attempt to bring down the SER, a few different alternatives to the conventional 6T SRAM cell have been suggested [7–15]. The most essential reinforcing method is via the process of building a new and unique architecture of transistor connections inner within cells. This is done in order to create circuit-level protection. The software error-resistant Quatro-10T type SRAM cell that was presented in [7], which provides differential read operation together with a wide noise margin, was developed by us. Whatever the case may be, it can only recover from "1" to "0," and as a result, it may not be totally resistant to SEU. Due of this feedback of the dual type node, which is known as the dual interlocked storage cell, or DICE [8] for short, it is possible that this single will not affect its immunity. The kind of temporary event known as SET, which takes place as a result of one of the nodes. Nonetheless, this basic capability of this kind SEMNU's immunity and the radiation hardness performance on this has yet seen an improvement. This is based on the trigger, and in [4] there was a proposal made for a trigger-based finfet (TBF)- 14T memory cell that was totally SEU immune, used less power, was faster, and had less latency. In contrast to mos sram 14t, the restricted marketing of this work, its qualities, and its capabilities is having a negative impact on the writing speed, the amount of power used, and the layout area. On the basis of this TBF-14T, two new types of radiation-hardened memory cells, designated radiation hardened already design (RHD)-11T and RHD-13T, were suggested in [9]. These memory cells had a higher degree of dependability. Yet, both their writing speed and write margin have worsened as a result of this change. Nevertheless, the authors employed nMOS as pull-up devices, which resulted in poorer read noise margins. The RH memory (RHM)-14T was presented in reference number 10, with the goal of obtaining low power and a truly highly dependable radiation-hardened application. Recent research published in [12] suggests that the RHD-14T memory cell has radiation hardness performance that is beneficial. In addition to the capability of tolerating a SEU on any of its internal single nodes, it may also offer the SEMNUs with some degree of immunological protection. Sadly, the application of it is limited because to the poor writing speed as well as the enormous amount of power that it consumes. Certain designing strategies have been presented as an alternate strategy for enhancing radiation tolerance [13], [14]. These techniques are in addition to the reinforcing at the circuit level, which has been the traditional method. The results of the hspice simulations will be analysed, and the layout optimization of the transistor pairs that are most susceptible to failure will be focused. The radiation-hardened with speed and power optimised (RSP)-14T bitcell is offered here as the result of this body of research effort. Its performance has been increased in comparison to that of a moss ram 14T cell thanks to the addition of two additional pMOS transistors that were used to strengthen redundant nodes.

In addition, since the branch where the redundant nodes are placed is supplied by the branch where the additional PMOSs are located, the feedback mechanism will be readily halted when the writing operation is taking place owing to this supply. As a result, both the write speed and the power consumption have seen significant improvements. In most cases, the radiation tolerance of the circuit is evaluated by the use of SPICE simulations by making use of the double exponential current source model. This method is efficient and saves time.

2. STATEMENT OF PROBLEM

SRAM cells, which are also called as static random access memory cells, have shown a radiation hardening issue in free space. For several types of SRAM cells, such as 6T, 12T, and so on, nearly every sort of work has already been done. In this particular work proposal, what we are really attempting to perform is evaluate an SRAM cell that is based on a 14T MOS to an SRAM cell that is built on a 14 FINFET in order to locate an alternative that is more effective and trustworthy in terms of power efficiency and delay.

This research work investigates how circuits that are based on FinFETs, which are fin-type field-effect transistors. FinFETs are an emerging transistor technology that is likely to supplement bulk CMOS (complementary metal-oxide-semiconductor) at 22-

nm, offering interesting delay–power tradeoffs and power consumptions for 14T FINFET SRAM cells. The HSPICE simulator, which is based on 22nm technology, is now being used here.

3. IMPLEMENTATION OF PROPOSED WORK

In this project, we work on a 14T SRAM cell based on the basis article [1], which is a radiation resistant structure and is constructed using MOSFET and FinFET in 22nm Technology. Synopsys HSPICE is the name of the programme that we make use of. This suggested method utilises an appropriate low power design strategy, which will be applied to the circuit in order to get the desired results.

The following are some examples of low power design techniques:

• Standby mode:

– Some examples are sleep transistor insertion, clock gating, and the application of minimal leakage vectors

– Interfere with (slow down/disable) the functioning of the circuit. – Ignore the issue of active mode leakage.

• Active mode: circuit optimization – Examples include gate size and multiple Vdd/Vth – Respect circuit operations and time limitations – May be utilised to decrease active mode leakage

One possible circuit is shown in the following image:

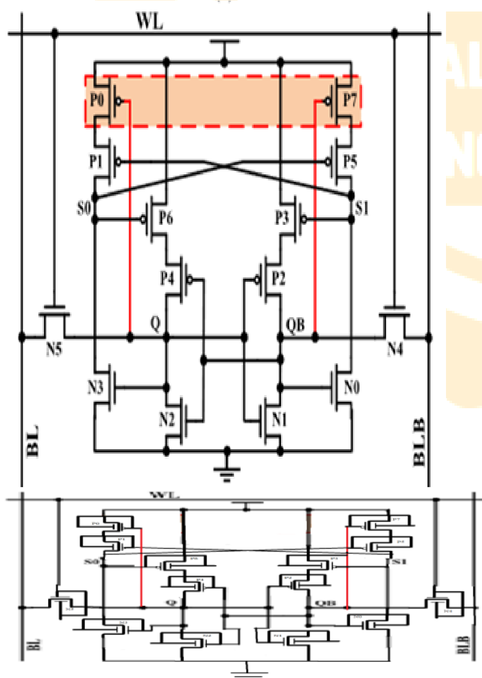

Fig.3: 14T MOS 14T SRAM cell and PROPOSED SG FinFET 14T SRAM cell

4. PROPOSED FINFET-BASED SRAM CELL

Due to the high number of single SRAM cell transistors, static random access memory, also known as SRAM, takes up a significant portion of the cell space in the designs of chips known as SOC [1]. Thus, in order to detect a high density, the SRAM cell generally has a tiny transistor size [2]. During the course of the last three decades, measurements using metal-oxide semiconductor field-effect transistor (MOSFET) technology have been employed to minimise the size of SRAM cells [3]. By decreasing the gate length, which ultimately results in a smaller SRAM cell, it is possible to execute an extra SRAM cell without increasing the trajectory, which ultimately results in an increase in memory retention capacity. Moreover, MOSFET depletion enhances SRAM performance at high transistor switch rates while simultaneously lowering the amount of power that is required [3]. Standard MOSFETs are beginning to fail owing to variable threshold voltage (VT) and short-term impact (SCE) as the technology moves closer and closer to 22 nanometers [4]. FinFET has been shown to be the most effective way for producing nanoscale MOSFETs, primarily because it allows the technical process to be slowed down to the 22 nm node [5, 6]. FinFET has a few benefits over MOSFET in a number of areas. To begin, FinFET is able to exert a greater degree of control over the station as a result of the presence of numerous operational gates [7]. As a consequence, FinFET has outstanding electrostatic characteristics [8]. In addition, superior FinFET gate control at the station helps to cut down on current source leakage, which in turn helps to squeeze more power out of the SCE. As a result, more FinFET reductions are attainable. In addition, a lightly doped FinFET channel lowers the random dopant variability, which in turn lowers the aka variability [9]. Pressure SCE and enhanced gate control over the channel make it possible to employ a large gate oxide and, as a result, greatly lower the amount of current that leaks from the gate oxide [10]. FinFET with a gate length of 14 nm is being put to its intended use since semiconductor manufacturing plans to employ it in the production of the next generation of products.

Procedures used in a diverse set of applications, namely SRAM in this particular instance. More SRAM cells may be inserted inside a single word (WL) line with each new upgrade in technological nodes that are introduced. When a multi-loaded design is used on a long wire, the integration power may be a significant contributor to the functioning of an SRAM cell, which is defined as the rise in the level of the line of text and the decline in the pre-charged location signal [11]. Because of the welding strength and resistance of the WL cable, the resistor-capacitor (RC) transmission is introduced into the WL input signal. In addition to this, the cable

connection size contributes to the introduction of an imbalanced and intolerable RC design for high-performance SRAM [2]. The performance of SRAM is hindered by parasitic RC [10]. As a direct consequence of this, the SRAM RC and the integration delay correction circuit are used in order to counteract the effects of operational deterioration [11]. On the other hand, there was no activity conducted on the implications of the RC delay in the SRAM output signal. The maximum amount of RC delay that an SRAM cell can accept before its functioning fails is not shown. The behaviour of an internal FinFET-based node that is based on 6T SRAM is evaluated for the very first time using a square wave input of varying RC delays, and it is discovered that an active SRAM cell has a little RC associated with it. The FinTET-based 6T SRAM cell strength and strength test in SPICE-direct current (DC) as well as interim analyses are looked at in this work. Analyzing SRAM storage, SRAM readings, and SRAM write functionality are the three components that are used to represent the Voltage (VTC) capability.

Inverter Model: SRAM is made up of two inverters that are connected in a closed loop and feed off of each other. A single inverter is studied such that gain, noise margin, and power dissipation may each be determined. The performance of the SRAM will be shown by the analysis of a single inverter. In Figure 4, we see the schematic for the DC analysis performed on the SRAM inverter. An examination of DC current is carried out at node q, and the voltage at node q is monitored..

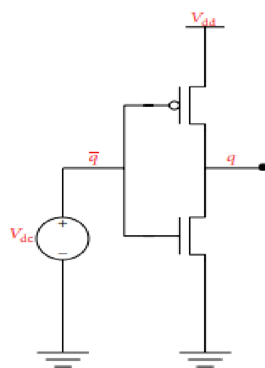

Fig4: Inverter Model

SRAM model: The HSPICE-based software is used to construct the SRAM cell. The SRAM cell model may be seen in Figure 3. V (WL) refers to the volume of the word line, V (BL) refers to the voltage of the line bar, and V (BLB) refers to the voltage of the line bit, while s1 and s0 are the internal SRAM nodes that each contain 1 bit. Logical 1 indicates that the voltage at node s1 is 1 V, whereas logical 0 indicates that the voltage at s0 is 0 V. This is because Vdd is 1 V. Setting up both BL and BLB is required before the number of internal nodes in SRAM can be read. The N5 and N6 transistors are also n-FinFET devices, and their function as accessibility transistors is to regulate access to the internal storage of the SRAM device during write and read operations. If the WL is validated, then both the N5 and the N4 will become accessible. The n-FinFET of the inverter is represented by the N1 and N3 nodes, while the p-FinFET is represented by the N2 and P4 nodes. It is important to note that both P2 and N1 are inverters. The data that is stored in the SRAM cell will remain in a stable state if the WL signal is not asserted.

5. RESULTS

A comparison of the MOS and FINFEt structures of an SRAM cell with regard to average power, delay, and PDP is shown here, and an analysis of the performance, speed, and area is carried out on the basis of the findings, which take into account numerous aspects.

a) Power Delay Product: The Product Delay (PDP) is defined as the product of total power dissipation and the amount of time it takes for an SRAM cell to be accessed. As a result of the fact that there is a trade-off between delays and energy consumption, the performance of an SRAM cell may be determined by calculating the product of energy delays (P. Upadhyay, 2015).

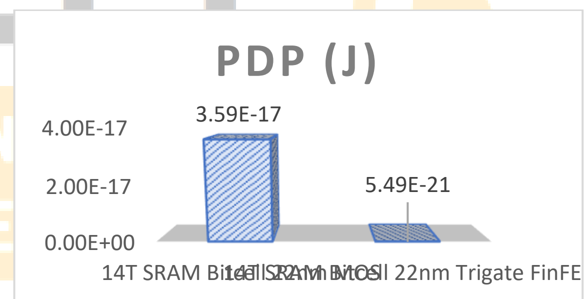

Fig a): Simulation graph of the proposed 14T SRAM FINFET and 14T SRAM MOS by HSPICE Power Delay Product (PDP)

b)Average Power: The amount of power that an SRAM device consumes and the heat it generates is one of the most important performance metrics [11]. The failure of the MOSFET-based SRAM to function when it is scaled down to the nanoscale regime of technology node results in the SRAM cell having a high power consumption and dissipation rate. In a typical SRAM, there is only one word line, denoted by the letter w; but, in this one, we make use of two word lines, denoted by the letters w1 and w2, in order to get superior results.

$$PAverage = XPactive + (1 - X)stand \quad by \, (1)$$

X is how much time the signal is active.

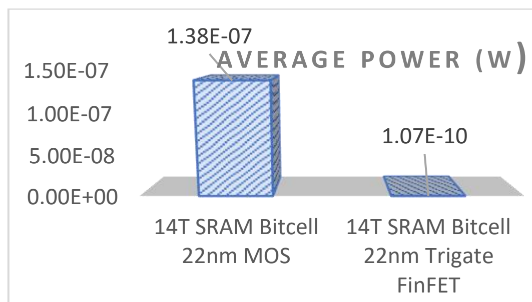

Fig. b): Simulation graph of the proposed 14T SRAM FINFET and 14T sram MOS by HSPICE average power (W)

c) Investigation of the Delay The delay of the SRAM cell may be quantified in terms of the delay of the circuit while it is being written to or read from. We get the write and read latency for a FinFET-based SRAM cell operating at 22nm and 14nm node technologies, respectively. Once again, the trade-offs within the system between powers, area, and delay are investigated here. The amount of time that passes between an input IN and an output OUT of the gate. Cadence spectrum calculator is being used in this delay analysis to compute the amount of time it takes for the state of the output to change whenever the state of the input changes.

$$tDelay = \frac{tpLH + tpHL}{2} \quad (1)$$

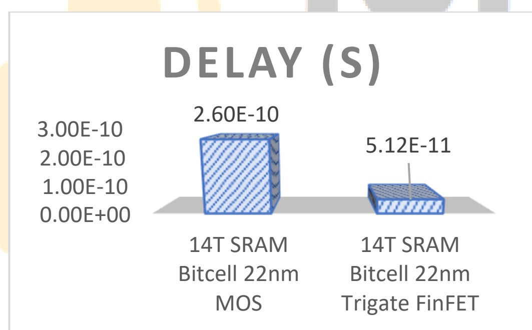

Fig. c): Simulation graph of the proposed 14T SRAM FINFET and 14T SRAM MOS by HSPICE delay

d) COMPARISON OF THE RESULTS:
Table i): shows the comparison of SRAM cells on the basis of different parameters:

	14T SRAM Bitcell 22nm MOS (base)	14T SRAM Bitcell 22nm Trigate FinFET (Proposed)
Average Power (w)	1.38E-07	1.07E-10
Delay (s)	2.60E-10	5.12E-11
PDP (J)	3.59E-17	5.49E-21
Voltage Source Power Dissipation (w)	1.43E-08	2.90E-11

6. CONCLUSION

In this article, a comparison is made between the MOS-based 14T SRAM cell at 22nm and the FinFET-based 14T SRAM cell at 22nm. The findings that were obtained for the SRAM spice models suggest that there is a possible solution for the problems that are associated with scaling MOSFETs. Based on the static noise margin values that were obtained for the SRAM cell, it was determined that a FinFET-based SRAM cell is reliable at lower technological nodes, and that the tolerated capacity is greater in the nanoscale regime. As may be seen in the table, our findings are rather favourable. And as the graphs demonstrate, our efforts have been fruitful. The amount of power that the device consumes has greatly lowered, and this memory cell might be integrated with any memory-based devices that need less power consumption. The speed of the memory circuits is also studied in terms of the write and read delay, which shows that the read and write speed has increased and the system trade-offs between power, PDP and delay are manageable. For example, the delay has increased at MOS-based 14T SRAM 22nm model, but the power and area have reduced significantly. This indicates that the system trade-offs can be managed.

REFERENCES

[1] Chunyu Peng et al., "Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application" 2018 IEEE

[2] Ajay N. Bhoj et al., "Design of Logic Gates and Flip-Flops in High-performance FinFET Technology" 2013 IEEE

[3] Farid Moshgelani et al., "Low Leakage MUX/XOR Functions Using Symmetric and Asymmetric FinFETs" international science index vol: no.4 2013

[4] khushboo mishra et al., "DESIGN DIFFERENT TOPOLOGY FOR REDUCTION OF LOW POWER 2:1 MULTIPLEXER USING FINFET IN NANOMETER TECHNOLOGIES" International Journal of Nanoscience Vol. 12, No. 4 2013

[5] V Narendar et al., "Design of High-performance Digital Logic Circuits based on FinFET Technology" International Journal of Computer Applications (0975 – 8887) Volume 41– No.20, March 2012

[6] Zhichao Lu et al., "Short-Channel Effects in Independent-Gate FinFETs" IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 2, FEBRUARY 2007

[7] saurabh khandelwal et al., "Leakage Current And Dynamic Power Analysis Of Finfet Based 7t Sram At 45nm Technology" The International Arab Conference on Information Technology ACIT'2013

[8] R.Rajprabu et al., "Battery Performance Analysis of CMOS and FinFET Logic" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 2, Issue 1 Mar. – Apr. 2013

[9] Junki Kato et al., "Circuit Design of 2-Input Reconfigurable Dynamic Logic Based on Double Gate MOSFETs with Whole Set of 16 Functions" Contemporary Engineering Sciences, Vol. 7, 2014

[10] Michael C. Wang et al., "Low Power, Area Efficient FinFET Circuit Design" Proceedings of the World Congress on Engineering and Computer Science Vol I 2009

[11] Neha Yadav et al., "Modelling and Performance Analysis of Various FinFET Based Design Techniques for XOR and XNOR Circuits at 45 Nanometer Regime" ISSUE 2 VOL 3, APR-MAY-2014